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- 008_CPU_MISC,JTAG
- 009_CPU_CFG,RSVD
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- 017_DDR4_SO-DIMM_1
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- 019_DDR4_****
- 020_CPU_PCH_CSI2,EMMC

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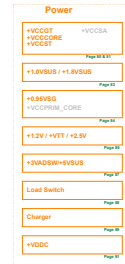
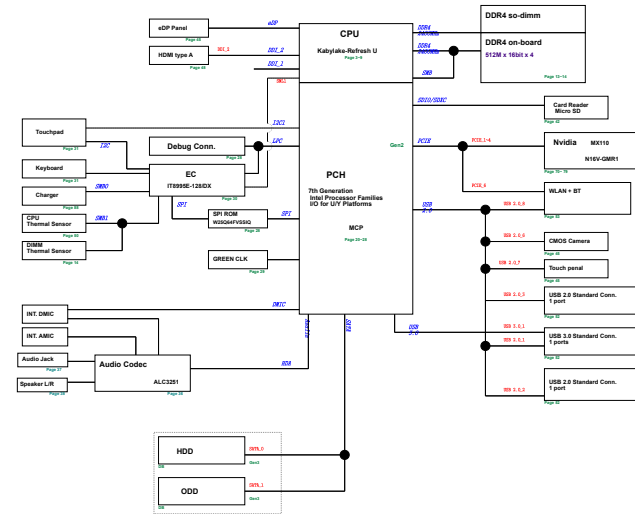
SYSTEM PAGE REF.

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019_DDR4_****	
020_CPU_PCH_CSI2,EMMC	

BLOCK DIAGRAM

X540UBR SCHEMATIC Revision 1.1

Non Connected Standby



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020_CPU_PCH_CSI2,EMMC

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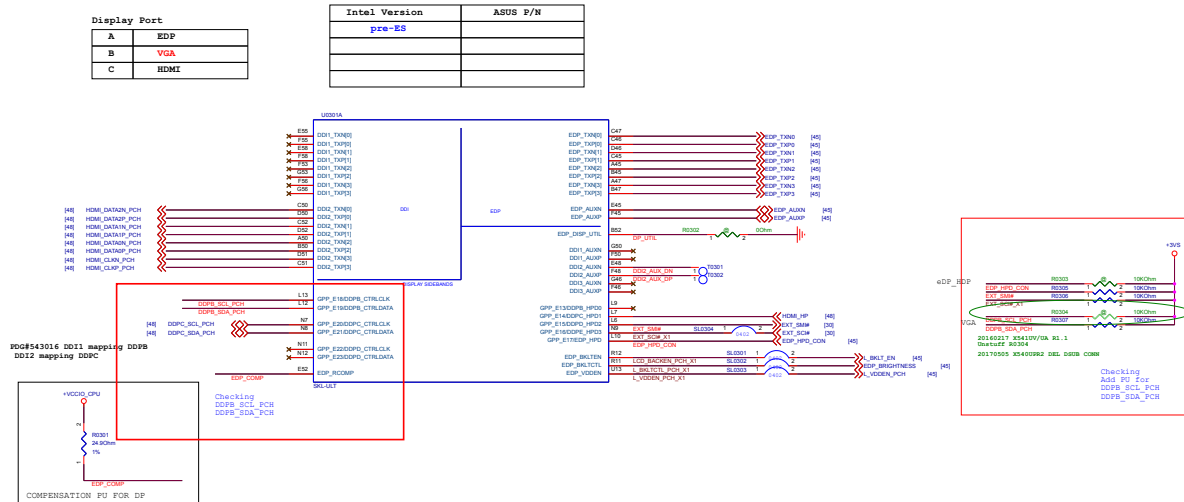
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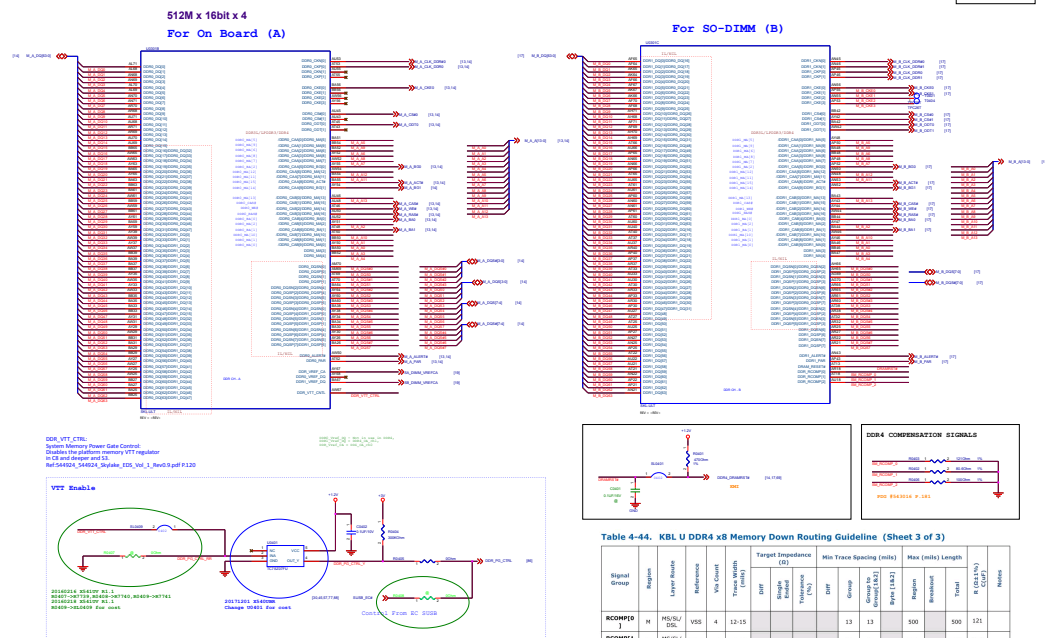


Table 4-44. KBL U DDR4 x8 Memory Down Routing Guideline (Sheet 3 of 3)

Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mil)	Target Impedance (Ω)		Min Trace Spacing (mil)		Max (mil) Length		R (dB/100)
						Single Impedance (%)	Differential	Group	Byes (14.4)	Region	Section	
RCONF0	H	HS/L/D6	V55	4	12-15			13	13	500	500	121
RCONF1	H	HS/L/D6	V55	4	12-15			13	13	500	500	80.6
RCONF2	H	HS/L/D6	V55	4	12-15			13	13	500	500	80.6

001 Block Diagram

002 System Setting

003 CPU DISPLAY

004 CPU DDR4

005 CPU LPC,SPI,SMB,CLINK

006 CPU POEWR

007 ***

008 CPU_MISC.JTAG

009 CPU CFG.RSVD

010 CPU POWER CAP

011 NB *****

012 NB *****

013 DDR4 TERMINATION A

014 DDR4 ON-BOARD A L32

015 DDR4 ON-BOARD A H32

016 DDR4 ****

017 DDR4 SO-DIMM 1

018.DDR4 CA VOLTAGE

019 DDR4 ****

020 CPU PCH CSI2.EMMC

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009_CPU_CFG,RSVD

010_CPU_POWER_CAP

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014_DDR4_ON-BOARD_A_L32

015_DDR4_ON-BOARD_A_H32

016_DDR4 ****

017_DDR4_SO-DIMM_1

018.DDR4_CA VOLTAGE

019_DDR4 ****

020_CPU_PCH_CSI2,EMMC

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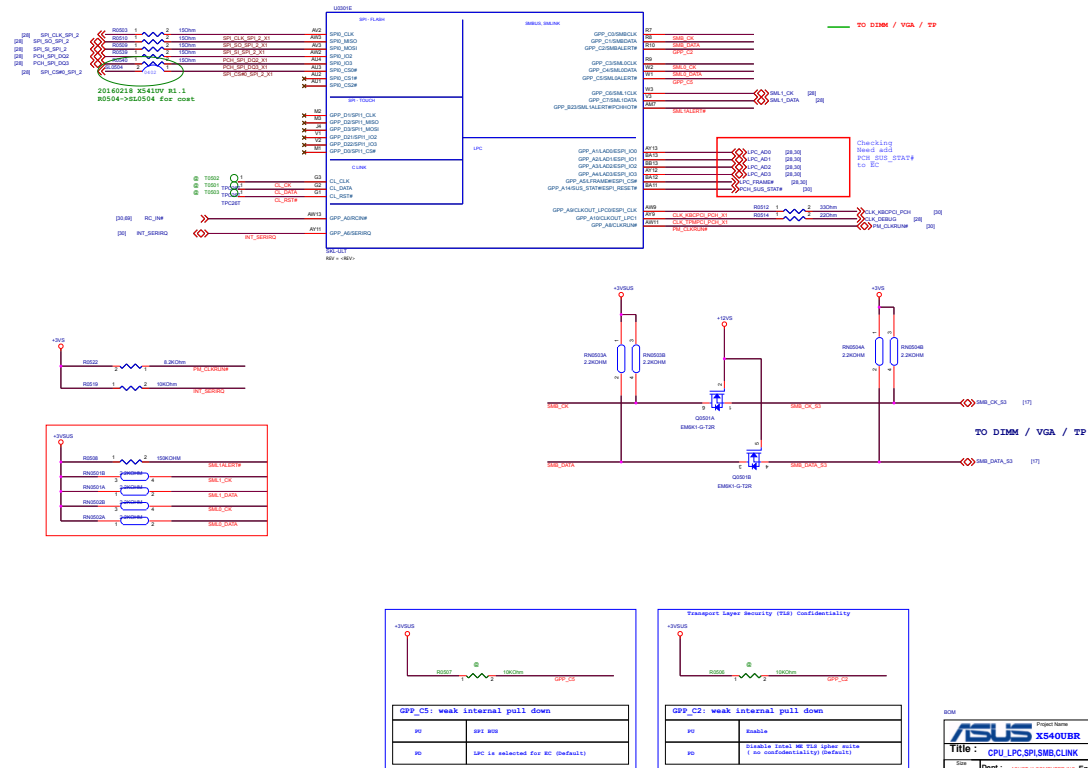
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ASUS		Project Name	Rev
Title: CPU LPC,SPI,SMB,CLINK			1.0
Dept.: ASUS COMPUTER INC. Engineer: NB_EE			
Date: Friday, March 16, 2018		Sheet	5 of 102

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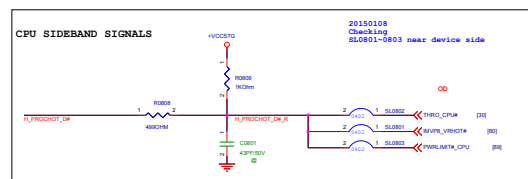
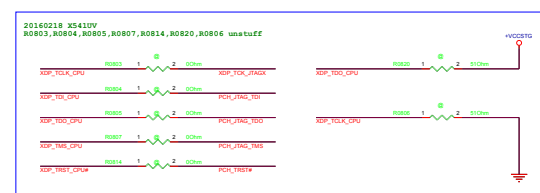
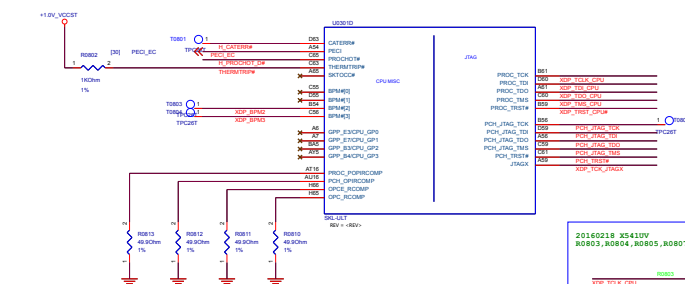
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019_DDR4_****

020_CPU_PCH_CSI2,EMMC

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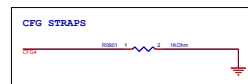
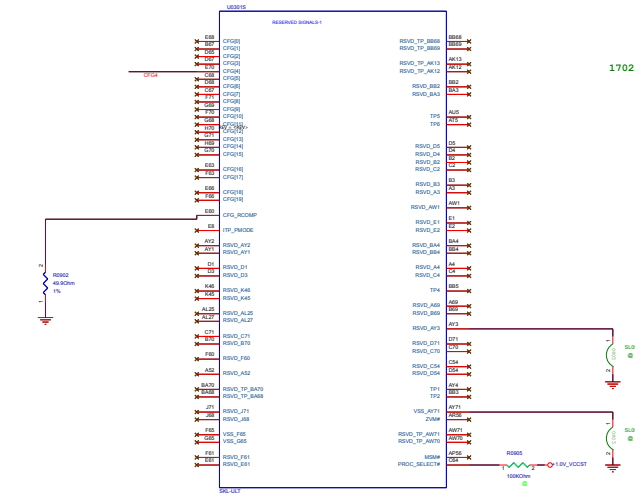
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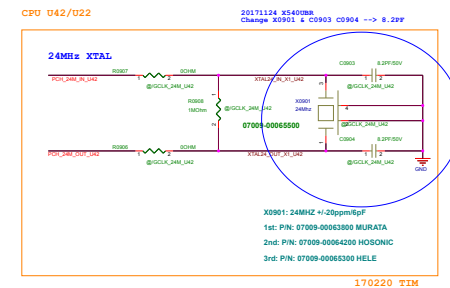
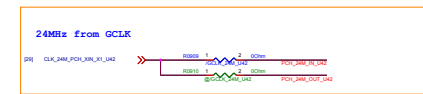
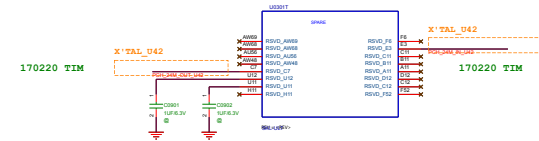
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	1	0	NOTE
CFG0	NO STALL	STALL	STALL RESET SEQUENCE AFTER PCU SILENCE UNTIL DE-ASSERTED
CFG4	DISABLE	ENABLE	eDP ENABLE



SCM	Project Name	Rev
ASUS	X540UBR	1.0
Title	CPU_CFG_RSVD	
Dept.	ASUSTeK COMPUTER INC. Engineer: NB_EE	
Date	Friday, March 16, 2018	Page 6 of 102

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- 014_DDR4_ON-BOARD_A_L32
- 015_DDR4_ON-BOARD_A_H32
- 016_DDR4_****
- 017_DDR4_SO-DIMM_1
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- 019_DDR4_****
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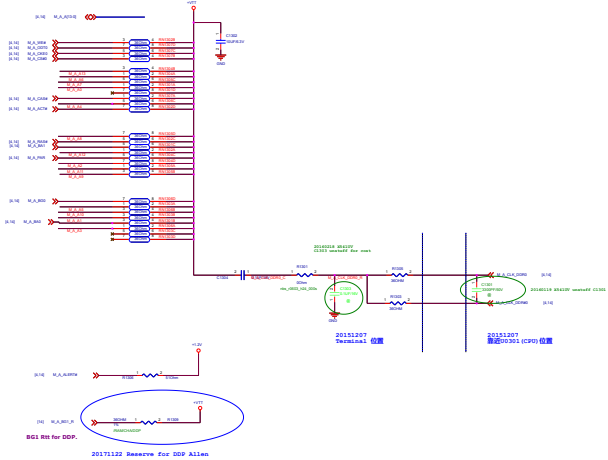


Table 4-2. System Memory Interface Guideline Terminology and Descriptions

SKL Processor and Memory Type	SKL H			
	DDR4/-RS SO-DIMM+ECC	DDR4/-RS SO-DIMM no ECC	DDR4/-RS Memory Down	LPDDR3 Memory Down
Signal Group Details				
Clock (CLK)	CKN[3:0], CKP[3:0]	CKN[3:0], CKP[3:0]	CKN[1:0], CKP[1:0]	CKP[1:0], CKN[1:0]
Control (CTRL)	CS#[3:0], ODT[3:0]	CS#[3:0], ODT[3:0]	CS#[1:0], ODT[1:0]	CS#[1:0], ODT[0]
Clock Enable (CKE)	CKE[3:0]	CKE[3:0]	CKE[1:0]	CKE[3:0]
Command (CMD)	W#E[14:0], BA[1:0], ACT#, PAR	W#E[14:0], BA[1:0], ACT#, PAR	W#E[14:0], BA[1:0], ACT#, PAR	CAA[9:0], CAB[9:0]
Strobe	DQS#P[7:0], DQS#N[7:0]	DQS#P[7:0], DQS#N[7:0]	DQS#P[7:0], DQS#N[7:0]	DQS#P[7:0], DQS#N[7:0]
ECC strobe	DQS#P[8], DQS#N[8]	N/A	N/A	N/A
Data	DQ[63:0]	DQ[63:0]	DQ[63:0]	DQ[63:0]
ECC Data	DQ[71:64]	N/A	N/A	N/A
Alert	ALERT#	ALERT#	ALERT#	N/A
Reset	DRAM_RESET#	DRAM_RESET#	DRAM_RESET#	N/A
RCOMP	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]

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006_CPU_POEWR

007_***

008_CPU_MISC,JTAG

009_CPU_CFG,RSVD

010_CPU_POWER_CAP

011_NB_****

012_NB_****

013_DDR4_TERMINATION_A

014_DDR4_ON-BOARD_A_L32

015_DDR4_ON-BOARD_A_H32

016_DDR4_****

017_DDR4_SO-DIMM_1

018_DDR4_CA VOLTAGE

019_DDR4_****

020_CPU_PCH_CSI2,EMMC

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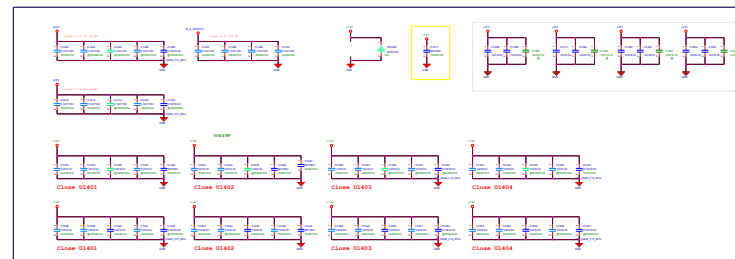
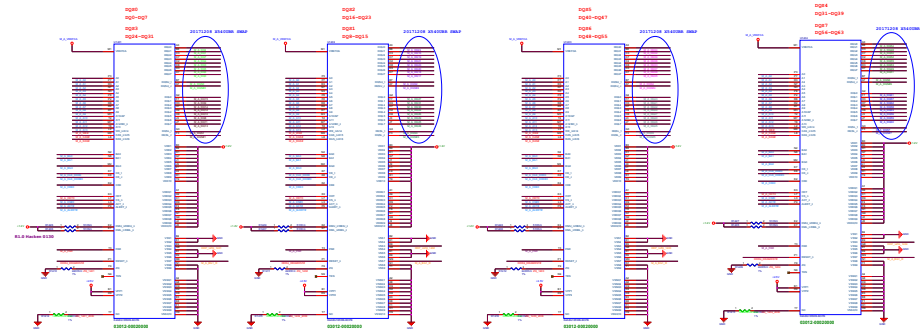
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Default Memory Settings		
Item	Value	Unit
DDR4 Frequency	2133	MHz
DDR4 Voltage	1.2	V
DDR4 Mode	Auto	



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U18.DDR4_CA VOLTAGE

019_DDR4_****

020_CPU_PCH_CSI2,EMMC

021_CPU_PCH_CGPIO, LPIO, MI
SC022_CPU_PCH_AUDIO,SDIO,SD
XC

023_CPU_PCH_PCIE,USB,SATA

024_CPU_PCH_CLOCK SIGNAL
S,RTC

025_CPU_PCH_SYS_POWER

026_CPU_PCH_POEWR,GND

027_CPU_PCH_POEWR,GND

028_PCH-SPI ROM,OTH,DEBUG

029_Silego_Green_CLK_Gen____

030_IT8995E-128/DX

031_KBC_KB,TP,KB-light

032_RST_Reset Circuit

033_

034_RTL8402_RJ45

035_****

036_AUD-ALC3251

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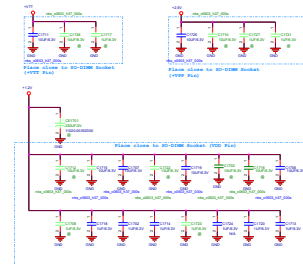
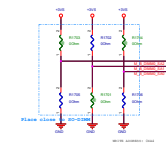
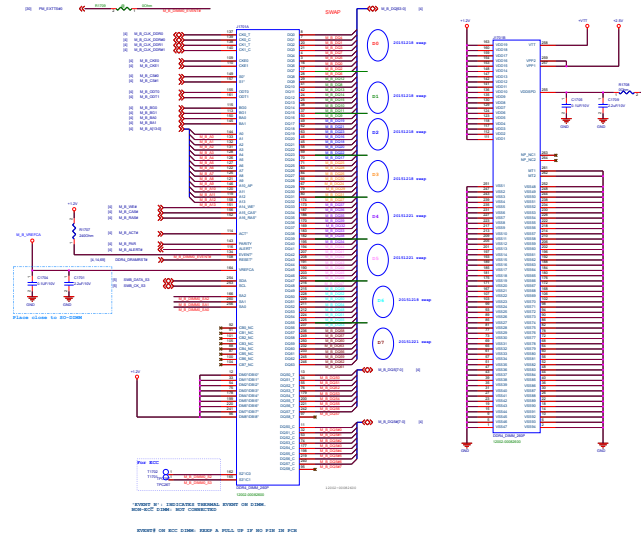
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018.DDR4_CA VOLTAGE

019_DDR4_****

020_CPU_PCH_CSI2,EMMC

021_CPU_PCH_CGPIO, LPIO, MI
SC022_CPU_PCH_AUDIO,SDIO,SD
XC

023_CPU_PCH_PCIE,USB,SATA

024_CPU_PCH_CLOCK SIGNAL
S,RTC

025_CPU_PCH_SYS_POWER

026_CPU_PCH_POEWR,GND

027_CPU_PCH_POEWR,GND

028_PCH-SPI ROM,OTH,DEBUG

029. Silego_Green_CLK_Gen____

030_IT8995E-128/DX

031_KBC_KB,TP,KB-light

032_RST_Reset Circuit

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034_RTL8402_RJ45

035_****

036_AUD-ALC3251

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Figure 4-51. SKL U DDR4/-RS x8 Devices Memory Down VREF-CA Overview

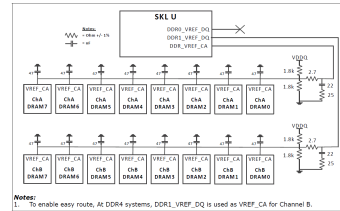
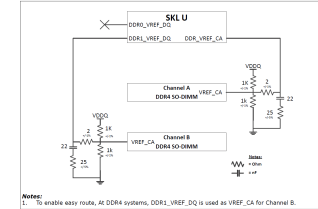
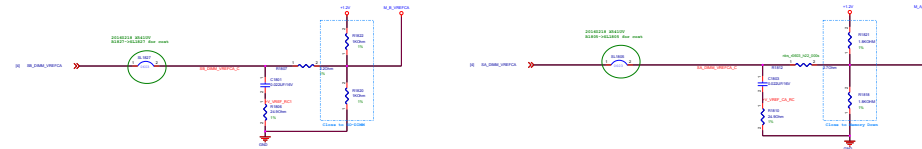


Figure 4-49. SKL U DDR4/-RS SODIMM VREF-CA Overview



All Vref trace must be 20 mils width



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019_DDR4_****

020_CPU_PCH_CSI2,EMMC

021_CPU_PCH_CGPIO, LPIO, MI
SC022_CPU_PCH_AUDIO,SDIO,SD
XC

023_CPU_PCH_PCIE,USB,SATA

024_CPU_PCH_CLOCK SIGNAL
S,RTC

025_CPU_PCH_SYS_POWER

026_CPU_PCH_POEWR,GND

027_CPU_PCH_POEWR,GND

028_PCH-SPI ROM,OTH,DEBUG

029_Silego_Green_CLK_Gen____

030_IT8995E-128/DX

031_KBC_KB,TP,KB-light

032_RST_Reset Circuit

033_

034_RTL8402_RJ45

035_****

036_AUD-ALC3251

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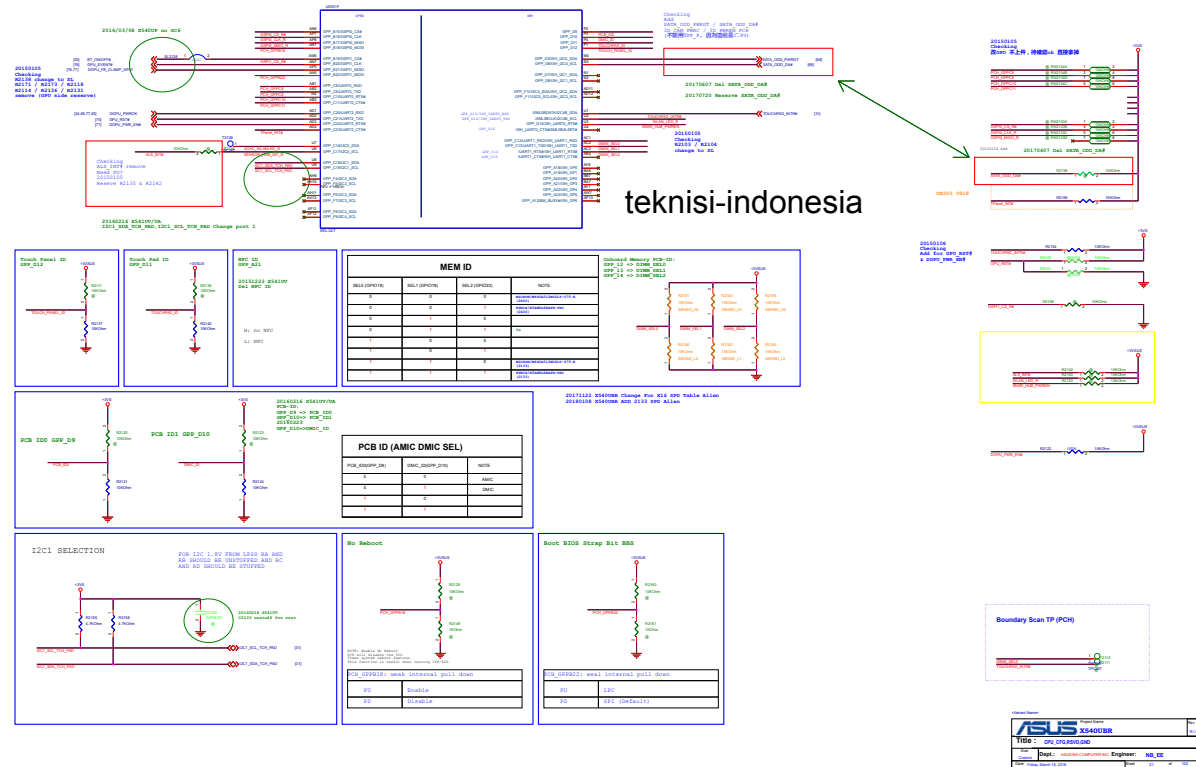
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019_DDR4_****

020_CPU_PCH_CSI2,EMMC

021_CPU_PCH_CGPIO, LPIO, MI
SC022_CPU_PCH_AUDIO,SDIO,SD
XC

023 CPU PCH PCIE,USB,SATA

024_CPU_PCH_CLOCK SIGNAL
S,RTC

025_CPU_PCH_SYS_POWER

026_CPU_PCH_POEWR,GND

027_CPU_PCH_POEWR,GND

028_PCH-SPI ROM,OTH,DEBUG

029. Silego_Green_CLK_Gen_____

030_IT8995E-128/DX

031_KBC_KB,TP,KB-light

032_RST_Reset Circuit

033

034_RTL8402_RJ45

035_****

036_AUD-ALC3251

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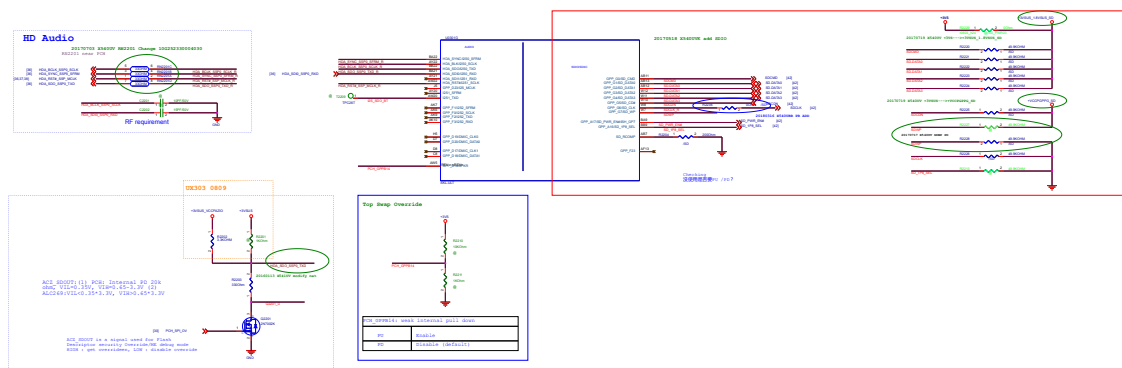
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019 DDR4 ****

020_CPU_PCH_CSI2,EMMC

021_CPU_PCH_CGPIO, LPIO, MI
SC022_CPU_PCH_AUDIO,SDIO,SD
XC

023 CPU PCH PCIE,USB,SATA

024_CPU_PCH_CLOCK SIGNAL
S,RTC

025_CPU_PCH_SYS_POWER

026_CPU_PCH_POEWR,GND

027_CPU_PCH_POEWR,GND

028 PCH-SPI ROM,OTH,DEBUG

029. Silego_Green_CLK_Gen_____

030_IT8995E-128/DX

031_KBC_KB,TP,KB-light

032_RST_Reset Circuit

033

034_RTL8402_RJ45

035_****

036_AUD-ALC3251

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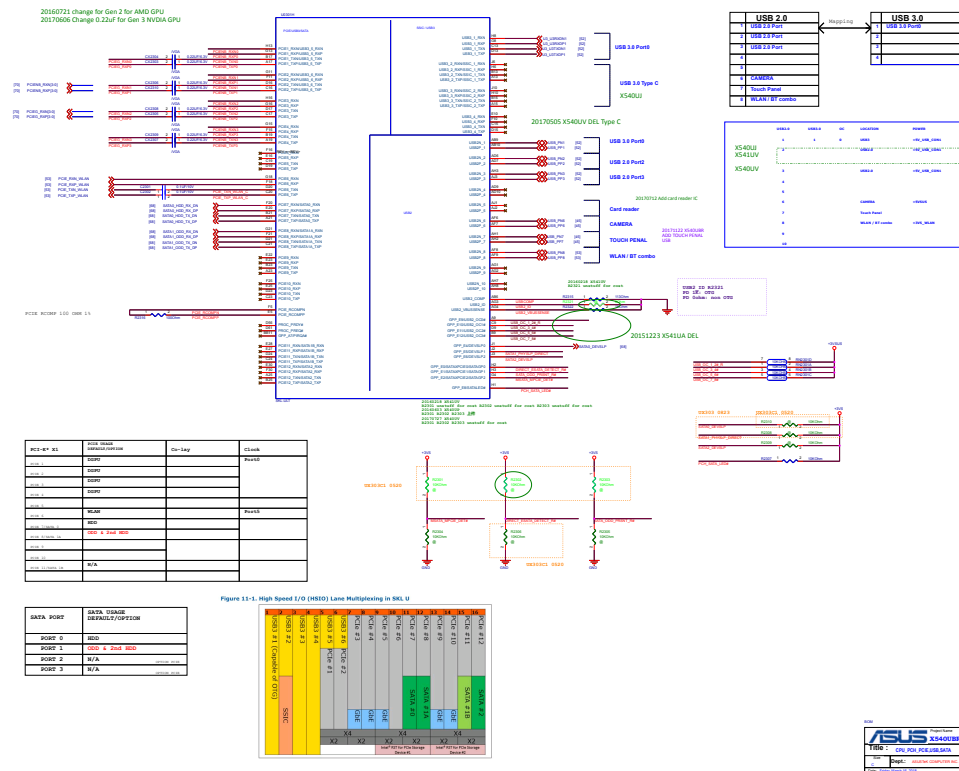


Figure 11-1. High Speed I/O (HSIO) Lane Multiplexing in SKL

REC#-REV#-SL	Price change description	Co-Lay	Class
REC# 1	START		Part 1
REC# 2	START		
REC# 3	START		
REC# 4	START		
REC# 5	START		
REC# 6	START		Part 1
REC# 7	START		
REC# 8	START		
REC# 9	START		
REC# 10	START		
REC# 11	START		
REC# 12	START		
REC# 13	START		
REC# 14	START		
REC# 15	START		
REC# 16	START		
REC# 17	START		
REC# 18	START		
REC# 19	START		
REC# 20	START		
REC# 21	START		
REC# 22	START		
REC# 23	START		
REC# 24	START		
REC# 25	START		
REC# 26	START		
REC# 27	START		
REC# 28	START		
REC# 29	START		
REC# 30	START		
REC# 31	START		
REC# 32	START		
REC# 33	START		
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REC# 37	START		
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REC# 90	START		
REC# 91	START		
REC# 92	START		
REC# 93	START		
REC# 94	START		
REC# 95	START		
REC# 96	START		
REC# 97	START		
REC# 98	START		
REC# 99	START		
REC# 100	START		

SATA PORT	SATA USAGE DEFAULT/OPTION
PORT 0	HD0
PORT 1	CD0 & 2nd HD0
PORT 2	N/A
PORT 3	N/A

 Project Name: X540UBR	
Title : CPU_POH_PCE_USB_SATA	
Date : 11/11/2015	Dept.: ASUSTek COMPUTER INC. Engineer: ND_CC

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- 021_CPU_PCH_CGPIO, LPIO, MI SC
- 022_CPU_PCH_AUDIO,SDIO,SD XC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNAL S,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029. Silego_Green_CLK_Gen____
- 030_IT8995E-128/DX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251

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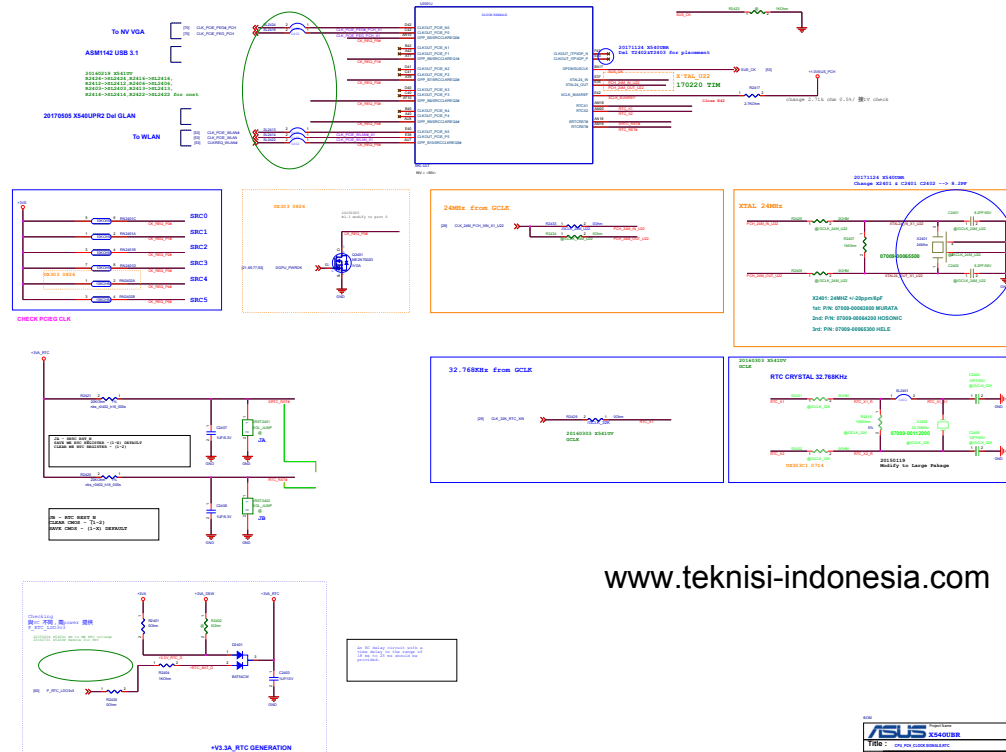
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SC022_CPU_PCH_AUDIO,SDIO,SD
XC

023 CPU PCH PCIE,USB,SATA

024_CPU_PCH_CLOCK SIGNAL
S,RTC

025_CPU_PCH_SYS_POWER

026_CPU_PCH_POEWR,GND

027_CPU_PCH_POEWR,GND

028_PCH-SPI ROM,OTH,DEBUG

029. Silego_Green_CLK_Gen_____

030_IT8995E-128/DX

031_KBC_KB,TP,KB-light

032_RST_Reset Circuit

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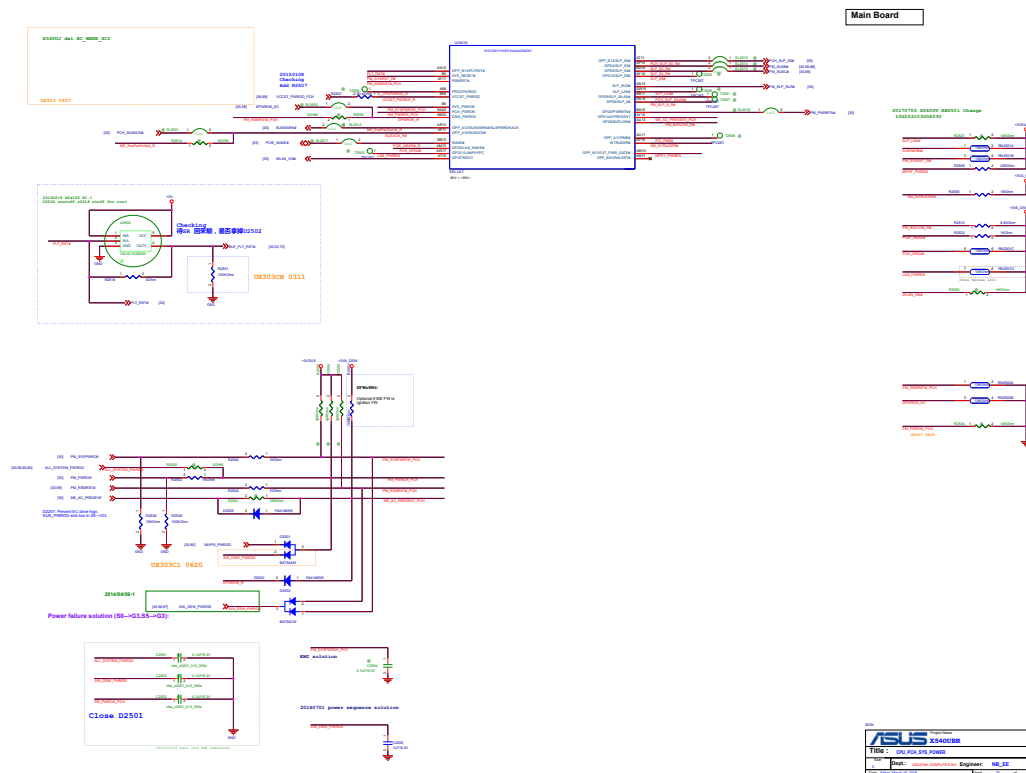
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SC022_CPU_PCH_AUDIO,SDIO,SD
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023 CPU PCH PCIE,USB,SATA

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S,RTC

025_CPU_PCH_SYS_POWER

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027_CPU_PCH_POEWR,GND

028_PCH-SPI ROM,OTH,DEBUG

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031_KBC_KB,TP,KB-light

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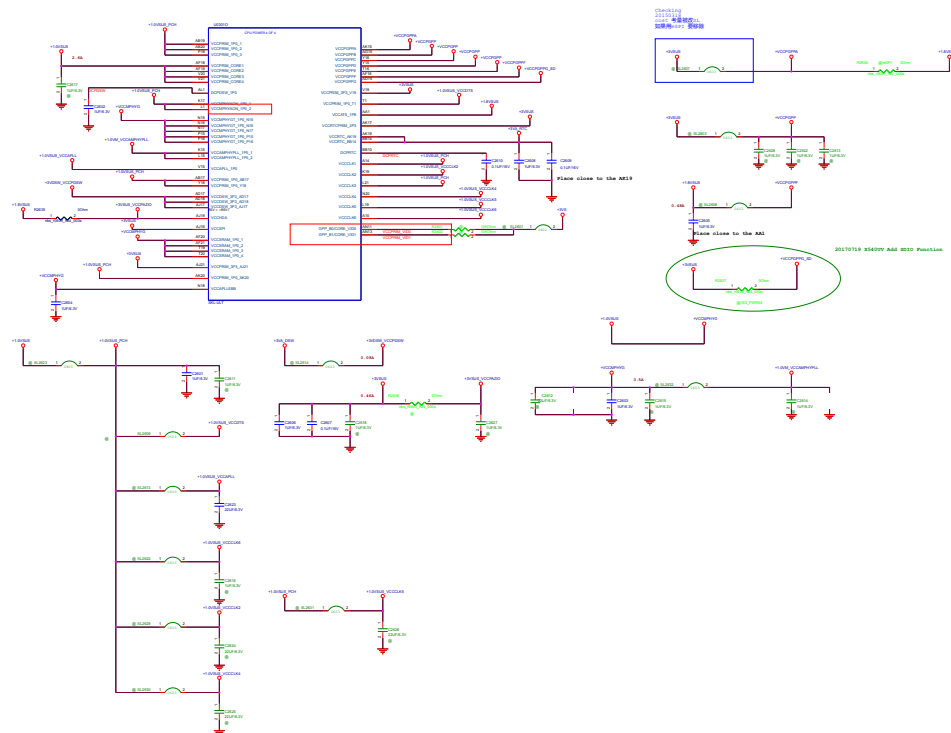
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S,RTC

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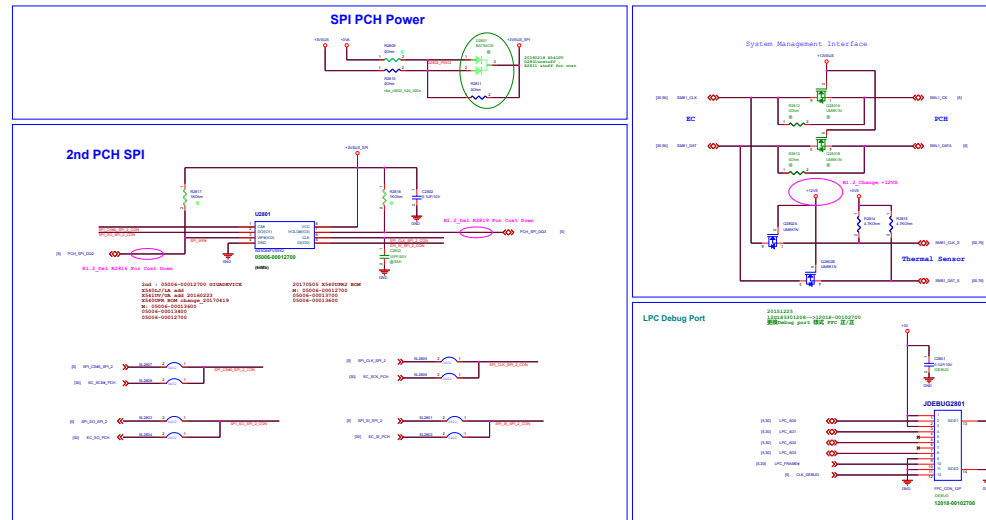
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048_HDMI-type A
049_
050_FAN_Thermal Sensor
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053_NGFF(KEY-E)_WLAN
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057_DSG_Discharge

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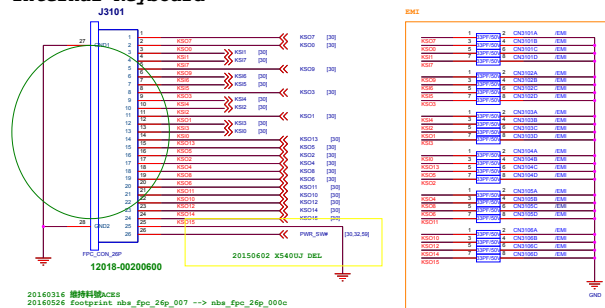
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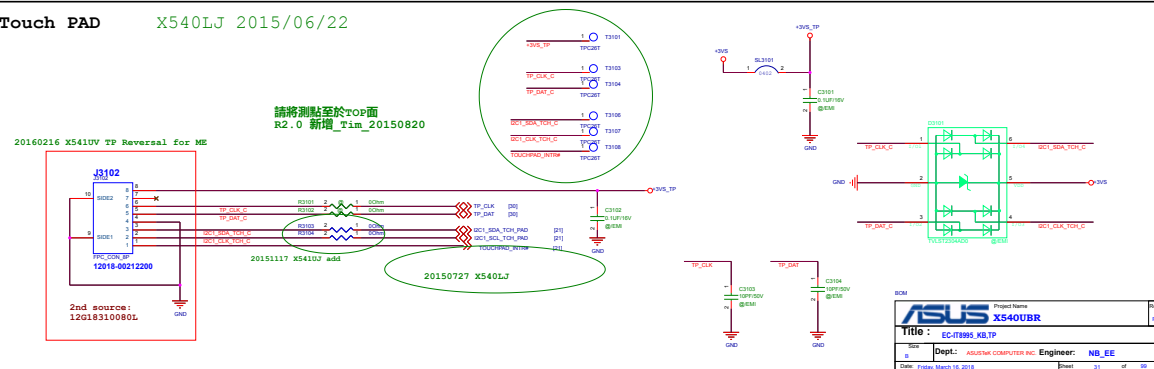
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Internal Keyboard



Touch PAD

X540LJ 2015/06/22



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047_eDP to VGA & CRT D-SUB

048_HDMI-type A

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050_FAN_Thermal Sensor

051_

052_USB 3.0 + 2.0 CONN.

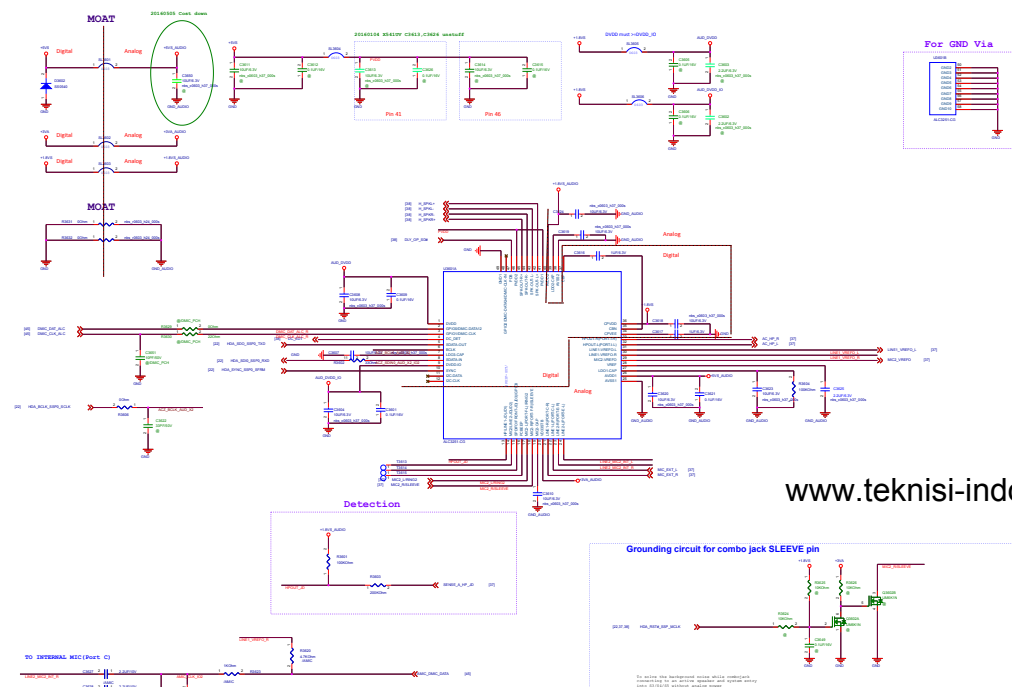
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056_***

057_DSG_Discharge



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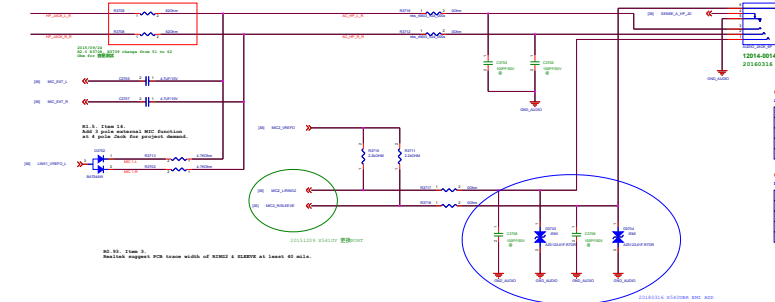
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Universal Jack (Normal open type)

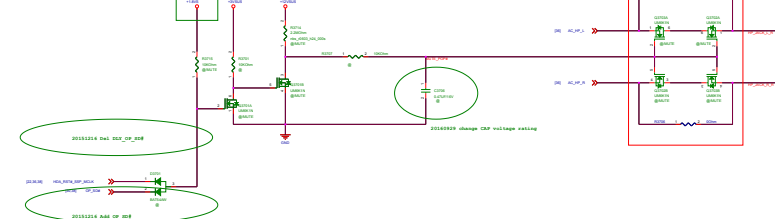
No. 3: Item 32.
Add a pin header jack signal
when type for product change.

No. 4: Item 33.
Reconnect the SP jumping resistance to pin for CR certification.
Reconnect the SP jumping resistance to pin for CR certification.
Reconnect the SP jumping resistance to pin for CR certification.



耳麦 mute mute

MUTE CONTROL



• 耳麦 - 一般性连接 (2 Pin, 3 Pin, 4 Pin)
• 耳机 - 一般性连接 (2 Pin, 3 Pin, 4 Pin)

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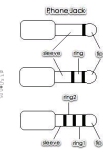
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CTIA - 通用接口				
Apple iPhone/iPad 通用接口				
Pin	Signal	Signal	Signal	Signal
1	Left channel	Left channel	Left channel	Left channel
2	Right channel	Right channel	Right channel	Right channel
3	Ground	Ground	Ground	Ground
4	Ground	Ground	Ground	Ground

OMT - 通用接口				
Apple iPhone/iPad 通用接口				
Pin	Signal	Signal	Signal	Signal
1	Left channel	Left channel	Left channel	Left channel
2	Right channel	Right channel	Right channel	Right channel
3	Ground	Ground	Ground	Ground
4	Ground	Ground	Ground	Ground



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047_eDP to VGA & CRT D-SUB

048_HDMI-type A

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050_FAN_Thermal Sensor

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052_USB 3.0 + 2.0 CONN.

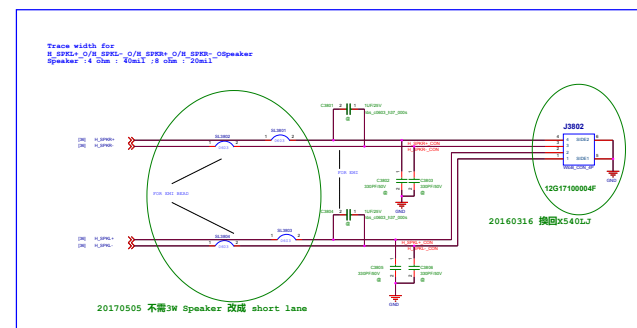
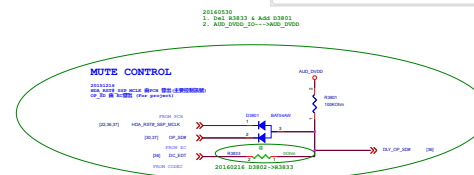
053_NGFF(KEY-E)_WLAN

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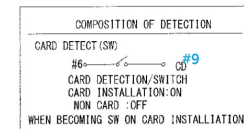
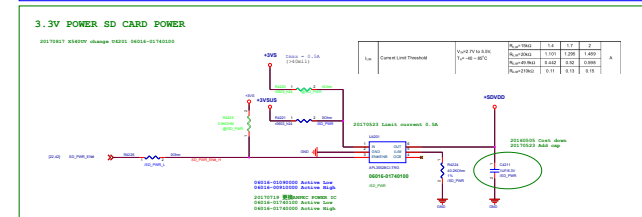
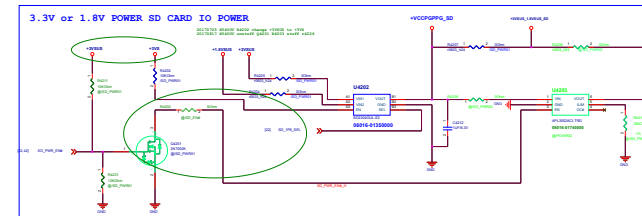
MoveTo

12023-00025900

Without card: CD/DE
Insert card (sdsc): CD/DE
Insert card (sdsc): CD/DE

PIN	SD mode
#1	DAT2
#2	DAT3/CD
#3	CMD
#4	V _{DD}
#5	CLK
#6	V _{SS}
#7	DAT0
#8	DAT1
CD	CARD DETECT

20170725 X5400V SD Power Condition
1. /SD_PWR0/SD_PWR02
2. /SD_PWR0/SD_PWR03-04207/SD_PWR02
3. /SD_PWR0/SD_PWR03-04207/SD_PWR03 ONLY 3.3V



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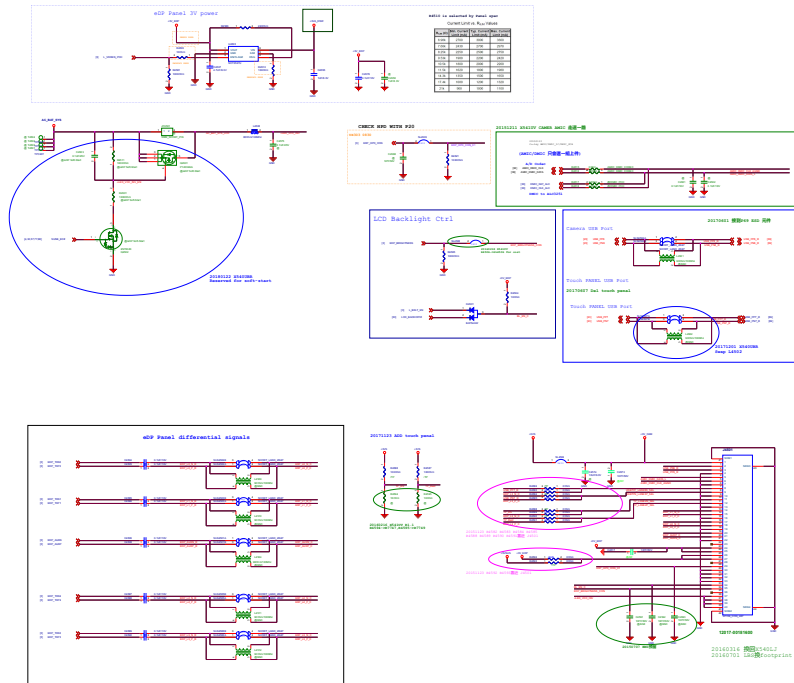
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eDP (LVDS) Panel



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048_HDMI-type A
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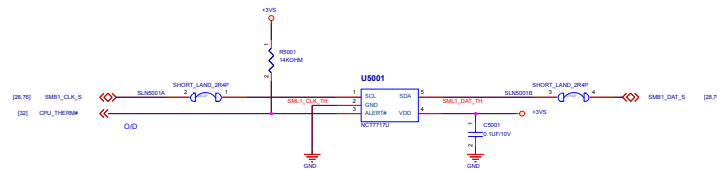
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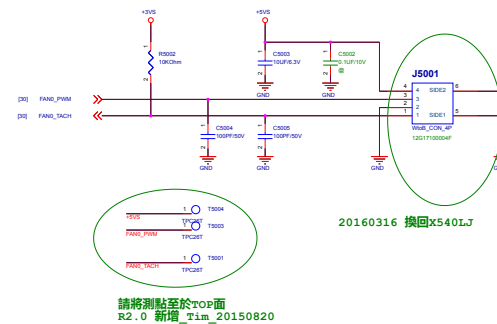
MoveTo

CPU Thermal Sensor



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DC FAN Control



請將測點至於TOP面
R2.0 新增 Tim_20150820

5.3 Address Setting

NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

5.6 ALERT# point hardware power-on setting (TBD)

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

PULL-UP RESISTOR		TEMPERATURE (°C)	
ALERT	2KΩ		75
	7.5KΩ		90
	10.5KΩ		100
	14KΩ		105
	18.7KΩ		110

Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

-----OTHER SIGNALS

10 mils

-----GND

10 mils

-----H_THERMDA(10 mils)

10 mils

-----H_THERMDC(10 mils)

10 mils

-----GND

10 mils

-----OTHER SIGNALS

Avoid FSB Power

Vibert Name:

ASUS		Title : NB_FAN_Thermal Sensor	
ASUSTeK COMPUTER INC.		Engineer: NB_EE	
Size	Project Name	Rev	
01	X540UBR	01.0	
Date	Friday, March 16, 2015	Draw	01 01 01

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052_USB 3.0 + 2.0 CONN.

053_NGFF(KEY-E)_WLAN

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056_***

057_DSG_Discharge

058_PRO_Protect

059_Power & WIFI & CAP LED&LI
D

060_DC_DC & BAT IN

061_****

062_

063_

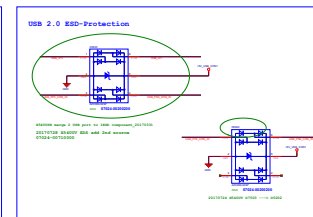
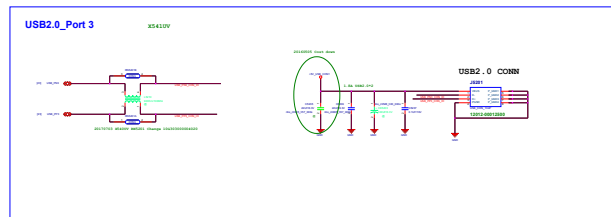
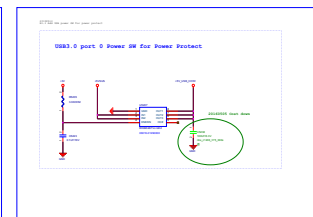
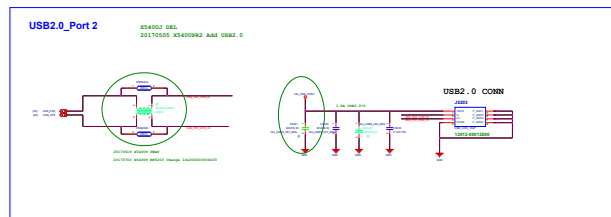
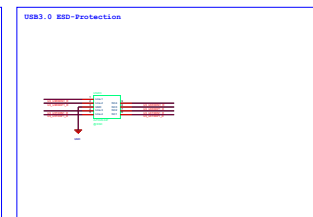
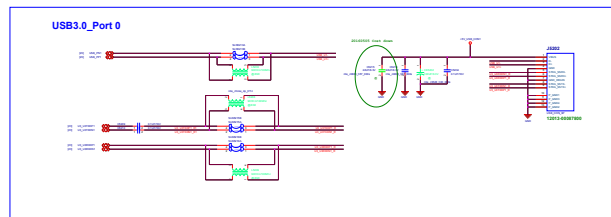
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065_ME_Conn & Skew Hole

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067_***

068_FFC connector_HDD_ODD



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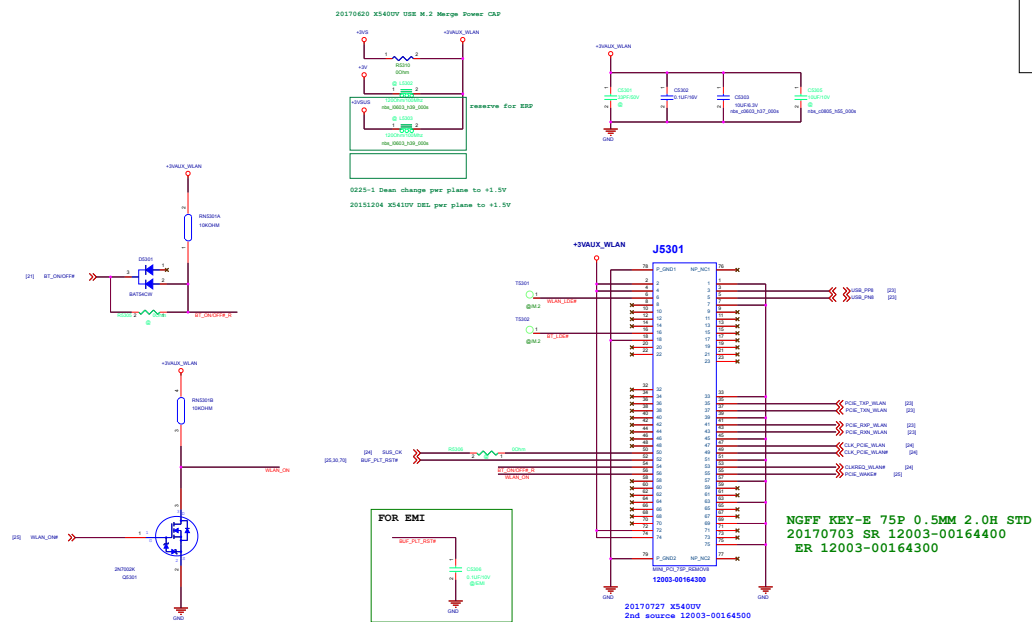
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Follow X540UBR
reverse wake on WLAN



NGFF KEY-E 75P 0.5MM 2.0H STD
20170703 SR 12003-00164400
ER 12003-00164300

20170727 X540UV
2nd source 12003-00164500

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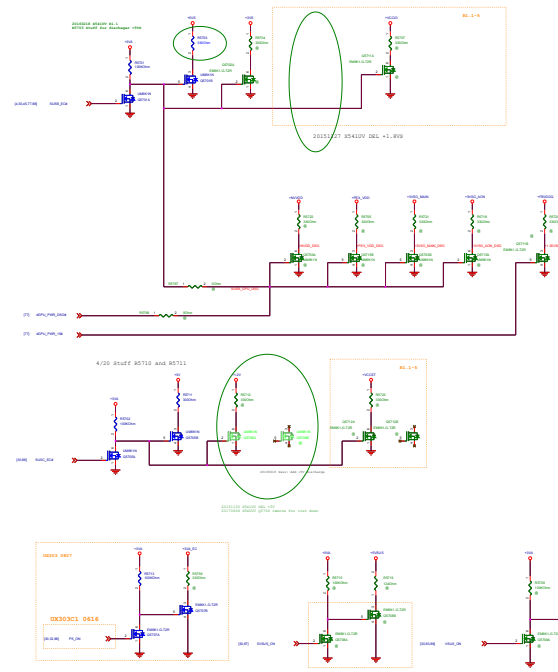
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Main Board



	
Project Name: XS400MR	
Title: DSG Discharge	
Dept: ASUSTek COMPUTER INC	Engineer: NG_SE

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053_NGFF(KEY-E)_WLAN
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058_PRO_Protect
059_Power & WIFI & CAP LED&LI
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065_ME_Conn & Skew Hole
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067_***
068_FFC connector_HDD_ODD

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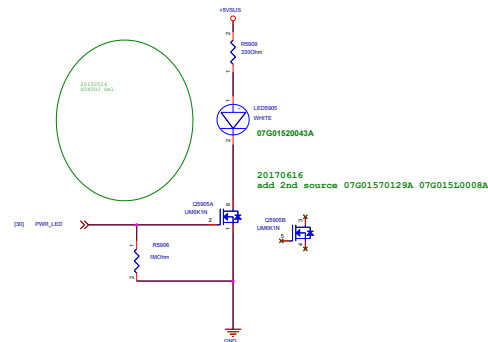
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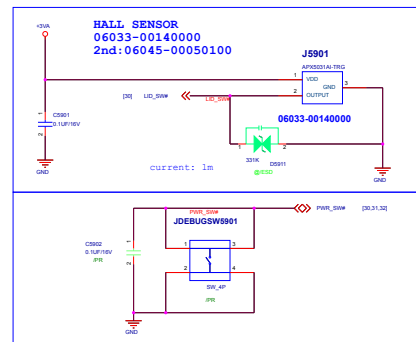
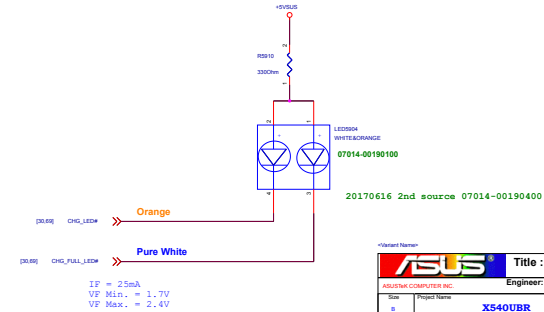
MoveTo

POWER LED



WIRELESS/ BT LED

CAP Lock LED

LED indicator
Charger LED

ASUS

ASUS		Title : 05_Power & WIFI & CAP LED	
ASUSTeK COMPUTER INC.		Engineer: NB_EE	
Site	Project Name	Rev	
01	X540UBR	01.0	
Date: 2016.03.10 10:00:00			

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- 065_ME_Conn & Skew Hole
- 066_
- 067_***
- 068_FFC connector_HDD_ODD

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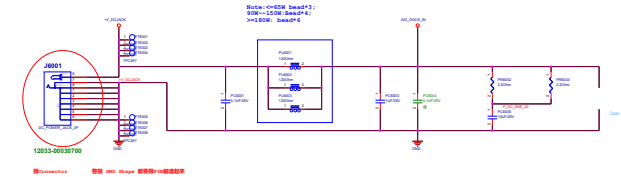
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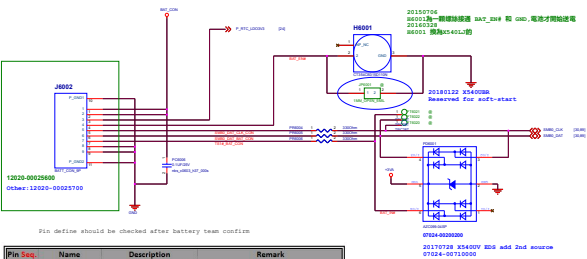
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Battery Connector



Pin define should be checked after battery team confirm

Pin	Symbol	Name	Description	Remark
1		P+	Battery pack positive terminal	Output voltage
2		P+	Battery pack positive terminal	Output voltage
3		LDO 3.3V		
4		EN#	External charge & discharge Master control pin	SYSTEM Connection to GND for charge & discharge
5		SMBC	Serial clock input	SMBC
6		SMBO	Serial data input	SMBO
7		BAT_IN#	EC detect battery_in pin	PACK inside 0 Ω connect to GND
8		P-	Battery pack negative terminal	GND
9		P-	Battery pack negative terminal	GND

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071_VGA_nVIDIA_N16V/S_FB-IF
072_VGA_nVIDIA_N16V/S_FB-GD
DR5
073_VGA_nVIDIA_N16V/S_VDD
074_VGA_nVIDIA_N16V/S_DISPL
AY
075_VGA_nVIDIA_N16V/S_ROM,
XTAL
076_VGA_nVIDIA_N16V/S_GPIO
077_VGA_nVIDIA_N16V/S_POWE

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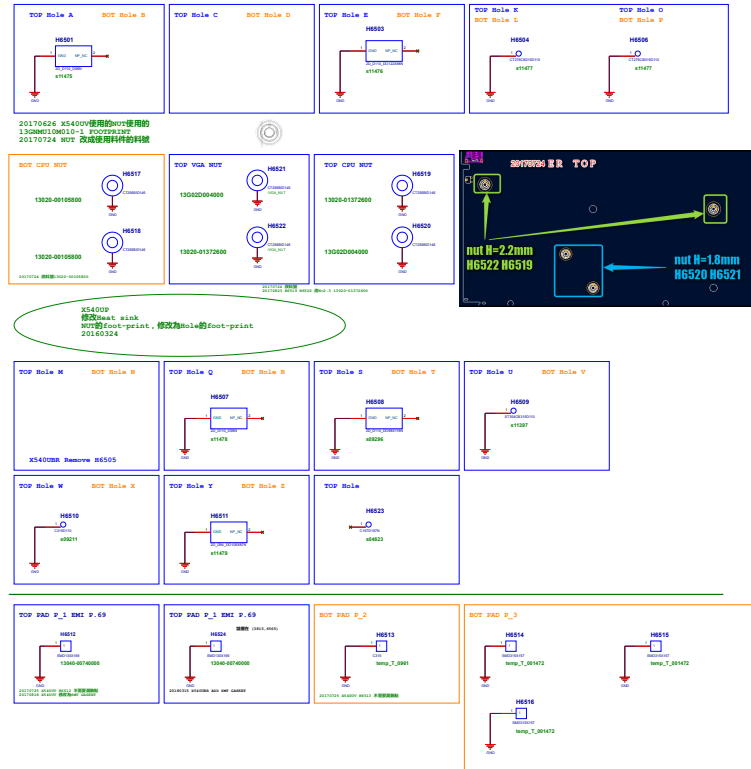
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075_VGA_nVIDIA_N16V/S_ROM,
XTAL

076 VGA nVIDIA N16V/S GPIO

077 VGA nVIDIA N16V/S POWE

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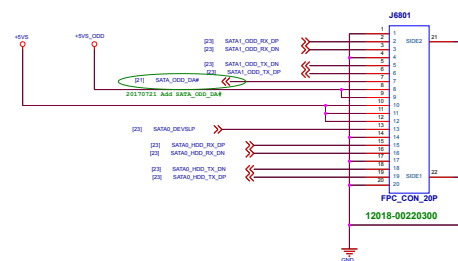
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MB to HDD_B

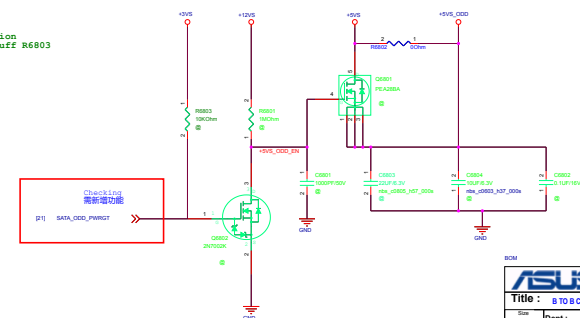
MB端 (MB to HDD B)

20150520 X540UJ



20160630 X541UAK/UVK follow X441 change FPC Connector
20170601 X540UV 20PIN FPC

```
20170720 X540UV Del
zero power ODD function
20170821 X540UV unstuff R6803
```



		Project Name			
		X540UBR			
Title : B to B CONNECTOR					
Size	Dept.: ASUS/TAI COMPUTER INC.		Engineer:	NB_EE	
Order	Order Date: March 15, 2015	Quantity	EA	rd	20

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AY
075_VGA_nVIDIA_N16V/S_ROM,
XTAL
076_VGA_nVIDIA_N16V/S_GPIO
077_VGA_nVIDIA_N16V/S_POWE

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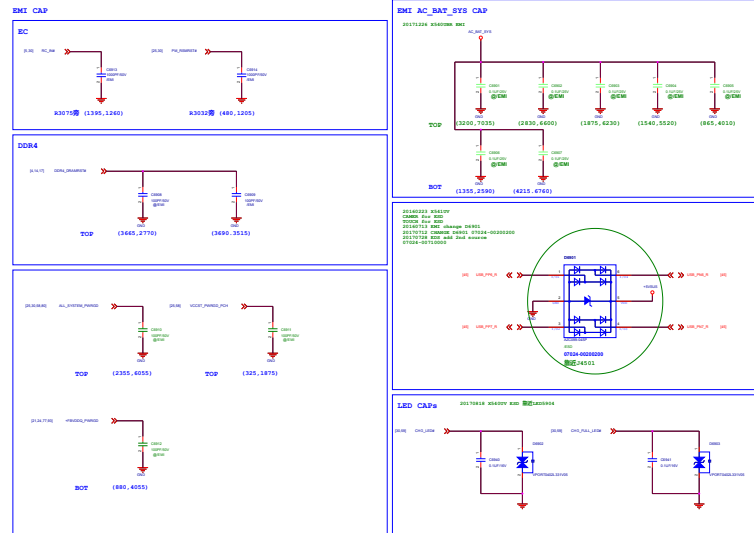
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075_VGA_nVIDIA_N16V/S_ROM,
XTAL

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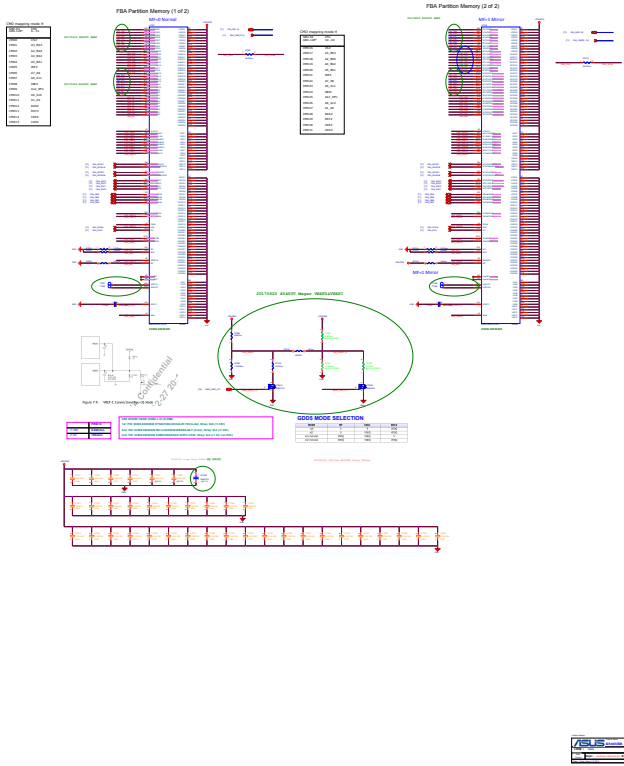
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069_EMI
070_VGA_nVIDIA_N16V/S_PCIE

071_VGA_nVIDIA_N16V/S_FB-IF
072_VGA_nVIDIA_N16V/S_FB-GD
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073_VGA_nVIDIA_N16V/S_VDD
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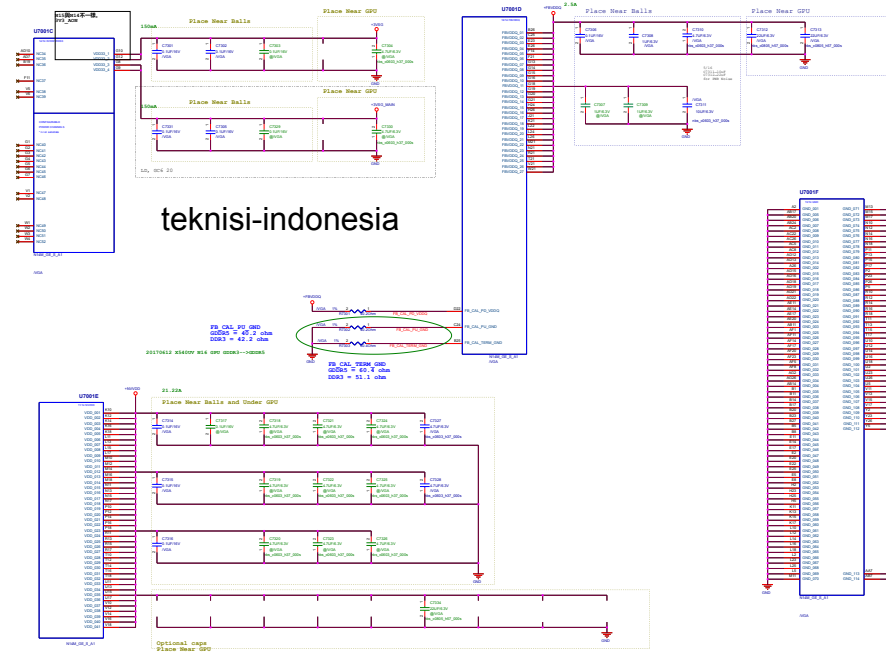
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XTAL

076_VGA_nVIDIA_N16V/S_GPIO

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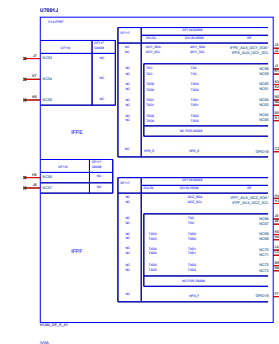
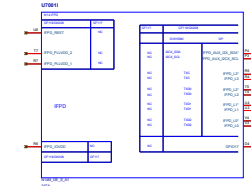
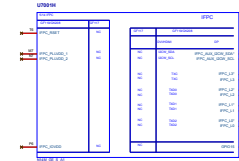
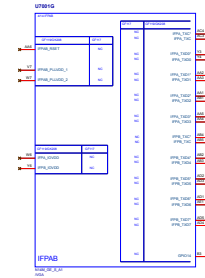
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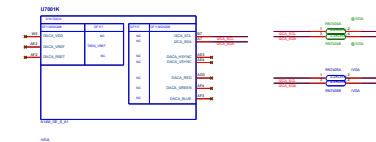
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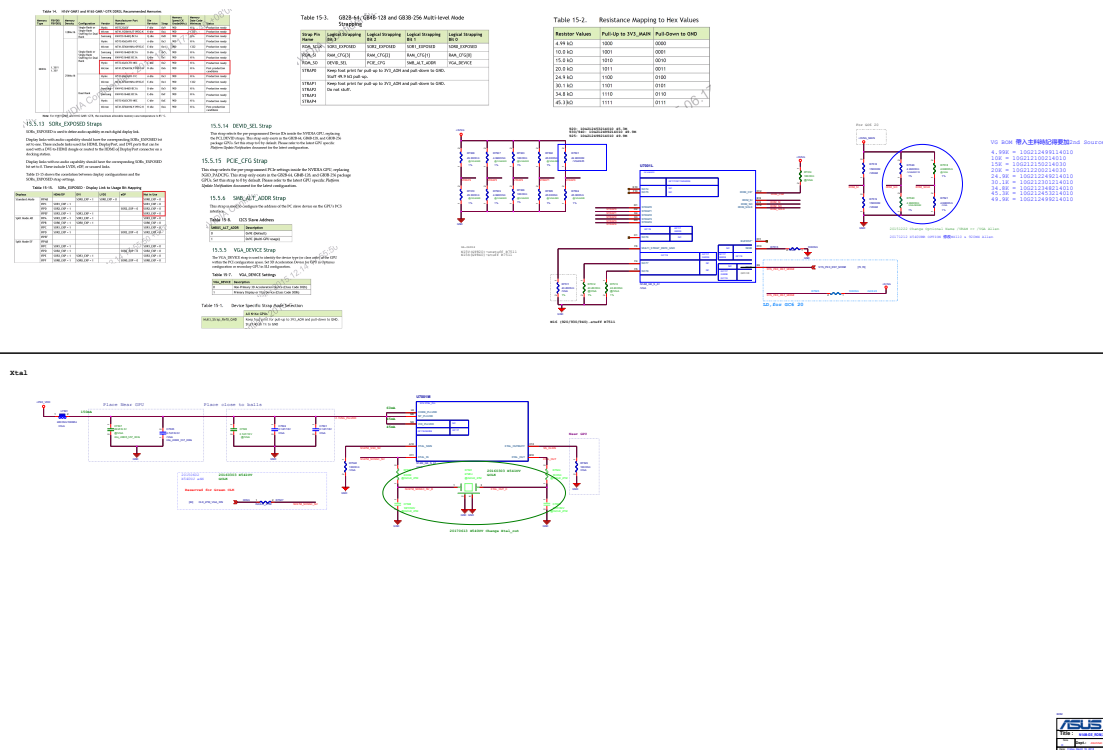
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AY075_VGA_nVIDIA_N16V/S_ROM,
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076 VGA nVIDIA N16V/S GPIO

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068_FFC connector_HDD_ODD

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070_VGA_nVIDIA_N16V/S_PCIE

071 VGA nVIDIA N16V/S FB-IF

072_VGA_nVIDIA_N16V/S_FB-GD
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073_VGA_nVIDIA_N16V/S_VDD

074_VGA_nVIDIA_N16V/S_DISPL
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075_VGA_nVIDIA_N16V/S_ROM,
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076 VGA nVIDIA N16V/S GPIO

077_VGA_nVIDIA_N16V/S_POWE

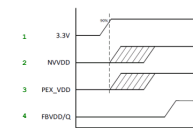
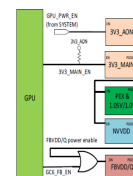
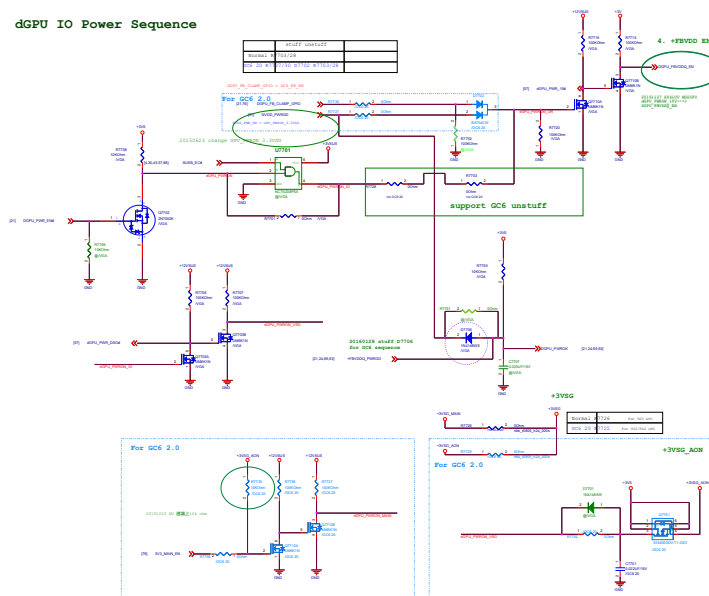
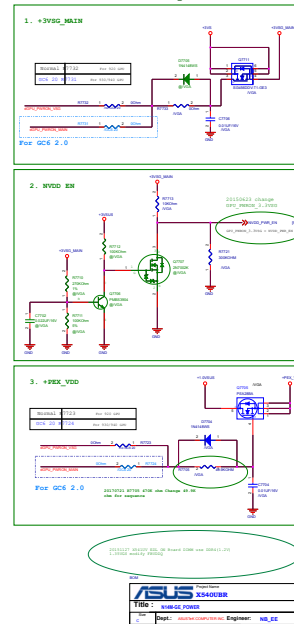


Figure 3-7. Example of Power-Up Sequencing Order

dGPU IO Power Sequence



dGPU Core Power Sequence



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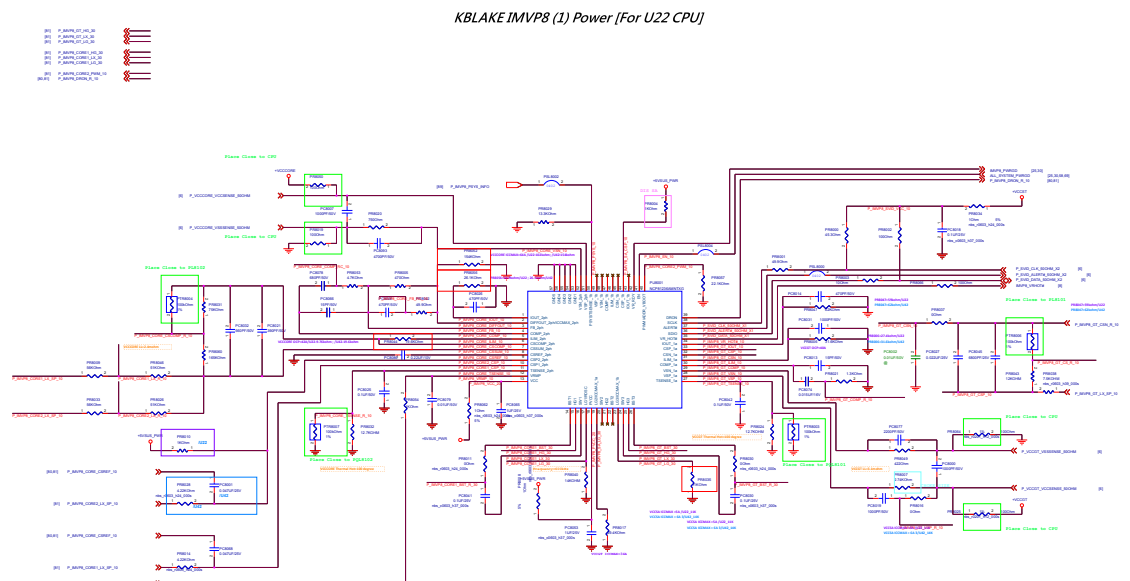
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AY

075_VGA_nVIDIA_N16V/S_ROM,
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076 VGA nVIDIA N16V/S GPIO

077_VGA_nVIDIA_N16V/S_POWE



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065_ME_Conn & Skew Hole

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068_FFC connector_HDD_ODD

069_EMI

070_VGA_nVIDIA_N16V/S_PCIE

071 VGA nVIDIA N16V/S FB-IF

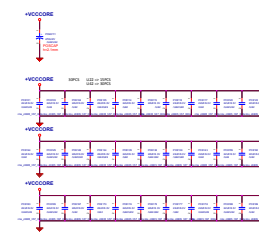
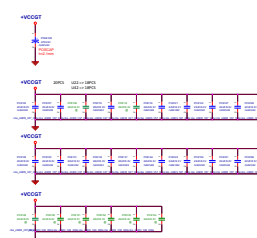
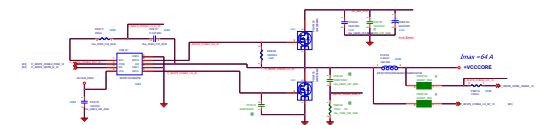
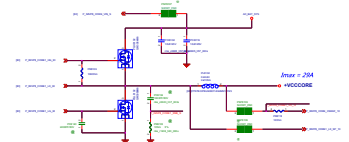
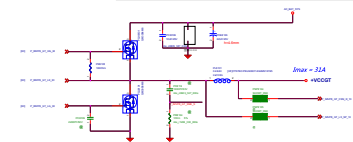
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083_PW_+1.0VSUS/+1.8VSUS
084_PW_
085_PW_***
086_PW_+1.2V/+VTT/+2.5V
087_PW_+3VADSW/+5VSUS
088_PW_LOAD SWITCH
089_PW_CHARGER
090_PW_PROTECTION
091_PW_+NVVDD (1)
092_PW_***
093_PW_+FBVDDQ

094_PW_***
095_PW_***
096_PW_***
097_PW_
098_PW_***
099_PW_FLOW CHART
100_Power On Timing--AC mode

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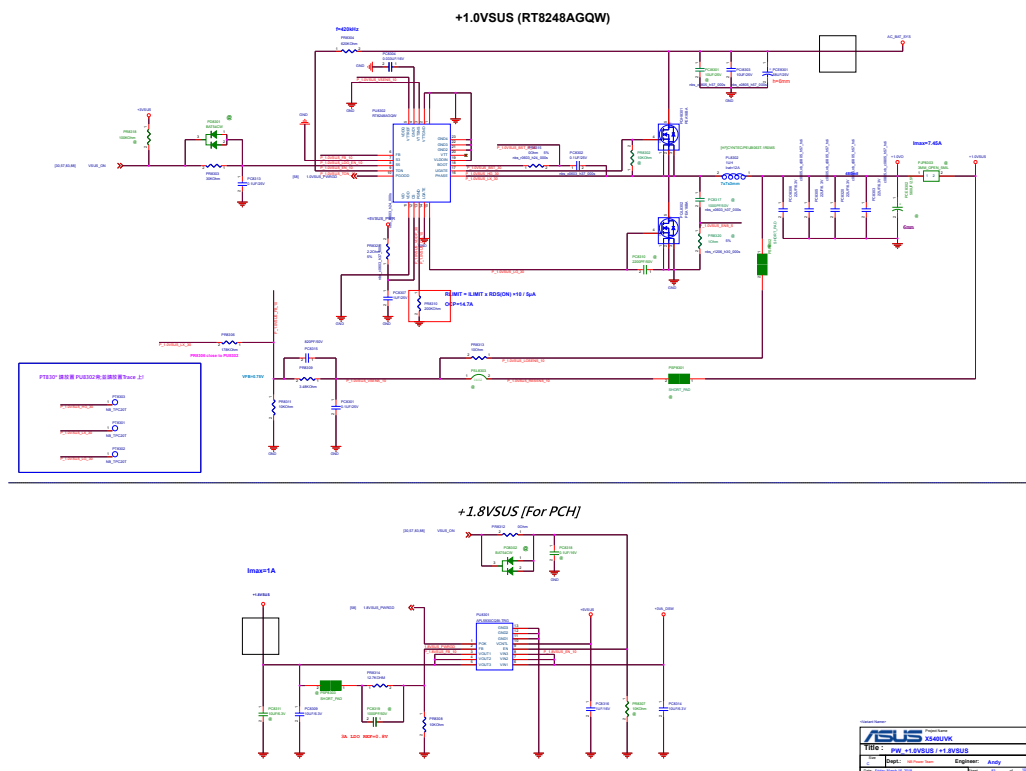
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081_PW_KABY LAKE-U42/U22(2)
082_PW_***
083_PW_+1.0VSUS/+1.8VSUS
084_PW_
085_PW_***
086_PW_+1.2V/+VTT/+2.5V
087_PW_+3VADSW/+5VSUS
088_PW_LOAD SWITCH
089_PW_CHARGER
090_PW_PROTECTION
091_PW_+NVVDD (1)
092_PW_***
093_PW_+FBVDDQ

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099_PW_FLOW CHART
100_Power On Timing--AC mode

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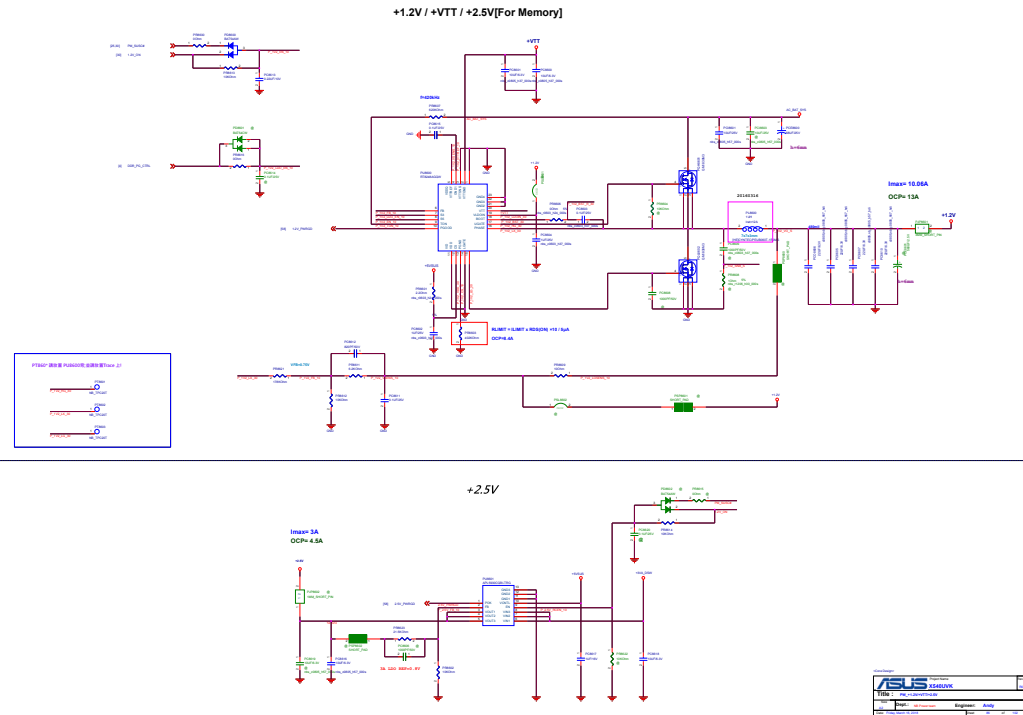
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081_PW_KABY LAKE-U42/U22(2)

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083_PW_+1.0VSUS/+1.8VSUS

084_PW_

085_PW_***

086_PW_+1.2V/+VTT/+2.5V

087_PW_+3VADSW/+5VSUS

088 PW LOAD SWITCH

089_PW_CHARGER

090_PW_PROTECTION

091_PW_+NVVDD (1)

092_PW_***

093_PW_+FBVDDQ

094_PW_***

095 PW ***

096_PW_***

097 PW

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099 PW FLOW CHART

100_Power On Timing--AC mode

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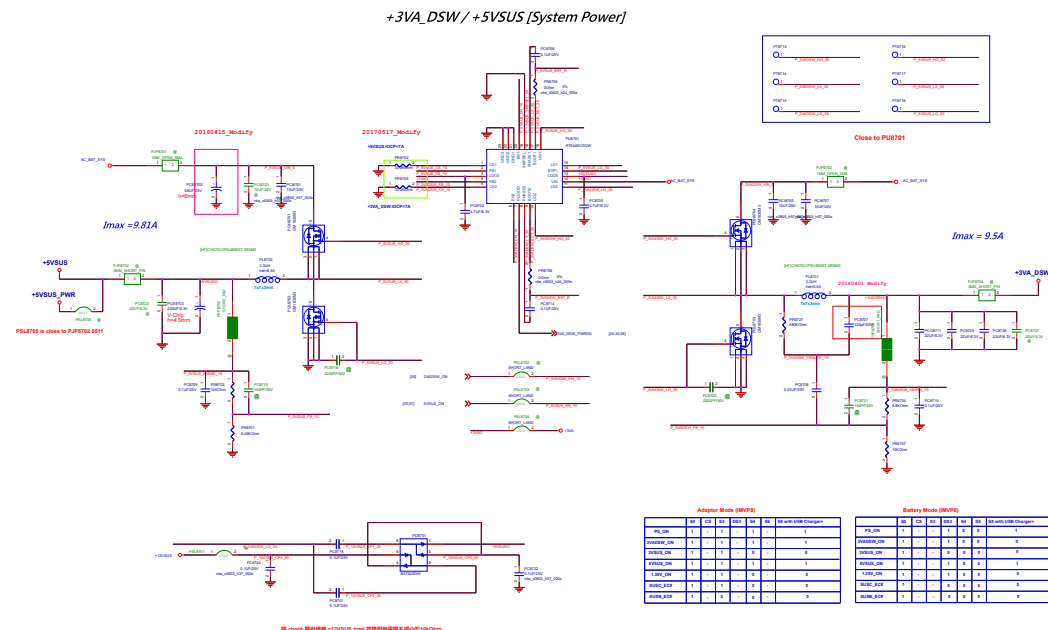
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teknisi-indonesia



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082_PW_***
083_PW_+1.0VSUS/+1.8VSUS
084_PW_
085_PW_***
086_PW_+1.2V/+VTT/+2.5V
087_PW_+3VADSW/+5VSUS
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100_Power On Timing--AC mode

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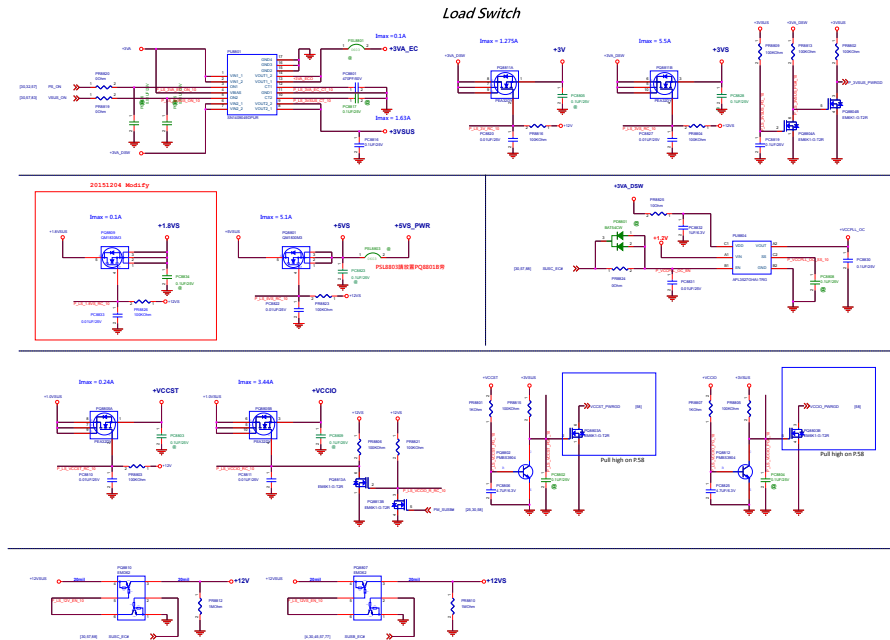
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ASUS X560VX	
Title : PW_LOAD_SWITCH	
Drawn: JH	Engineer: Andy
Check: JH	Rev: 1.0

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085_PW_***

086_PW_+1.2V/+VTT/+2.5V

087_PW_+3VADSW/+5VSUS

088 PW LOAD SWITCH

089_PW_CHARGER

090 PW PROTECTION

```
091 PW +NVVDD (1)
```

092 PW ***

093_PW_+FBVDDQ

094_PW_***

095 PW ***

096_PW_***

097 PW

098_PW_***

099 PW FLOW CHART

100_Power On Timing--AC mode

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086

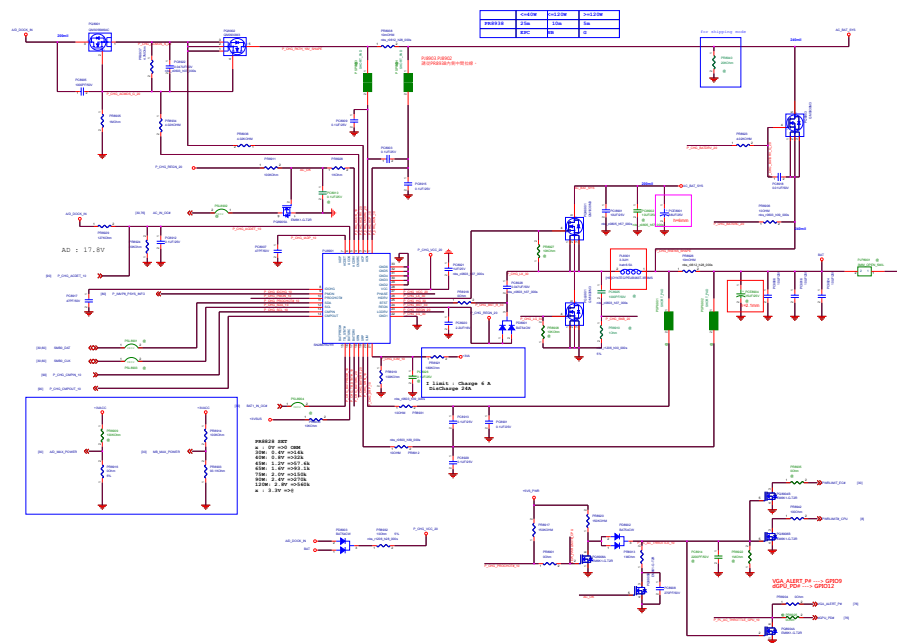
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080_PW_KABY LAKE-U42/U22(1)

081_PW_KABY LAKE-U42/U22(2)

082_PW_***

083_PW_+1.0VSUS/+1.8VSUS

084_PW_

085_PW_***

086_PW_+1.2V/+VTT/+2.5V

087_PW_+3VADSW/+5VSUS

088_PW_LOAD SWITCH

089_PW_CHARGER

090_PW_PROTECTION

091_PW_+NVVDD (1)

092_PW_***

093_PW_+FBVDDQ

094_PW_***

095_PW_***

096_PW_***

097_PW_

098_PW_***

099_PW_FLOW CHART

100_Power On Timing--AC mode

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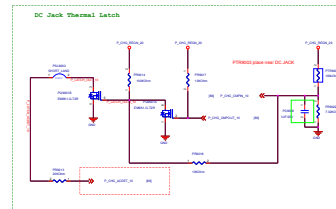
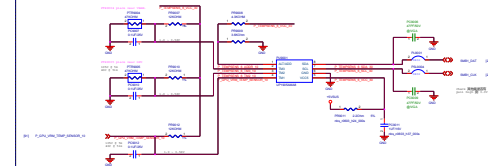
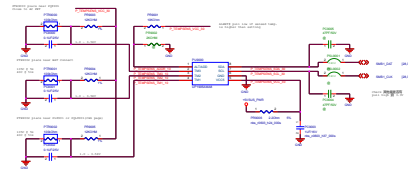
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Register Address							
ADDRESS	DATA	DATA	DATA	DATA	DATA	DATA	DATA
0x7F	0	0	0	0	0	0	0
STATUS	Temp. sensor threshold setting			Maximum Temp. delta			0000 0x0 0001 0x0 0002 0x0 0003 0x0
							0004 0x0 0005 0x0 0006 0x0 0007 0x0

ADDRESS	DATA	DATA	DATA	DATA	DATA	DATA	DATA
000000	00	0.75	00	0.50	0.50	0.50	0.50
000001	0000	0.00	0.50	0.50	0.50	0.50	0.50



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081_PW_KABY LAKE-U42/U22(2)
082_PW_***
083_PW_+1.0VSUS/+1.8VSUS
084_PW_
085_PW_***
086_PW_+1.2V/+VTT/+2.5V
087_PW_+3VADSW/+5VSUS
088_PW_LOAD SWITCH
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090_PW_PROTECTION
091_PW_+NVVDD (1)
092_PW_***
093_PW_+FBVDDQ
094_PW_***
095_PW_***
096_PW_***
097_PW_
098_PW_***
099_PW_FLOW CHART
100_Power On Timing--AC mode

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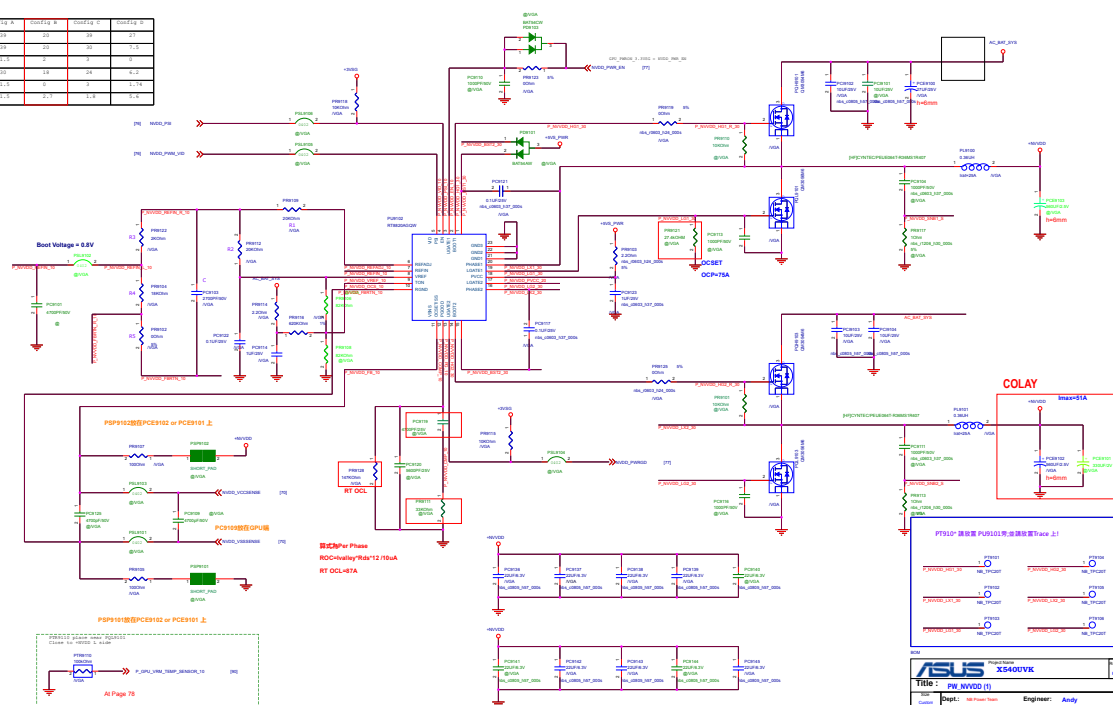
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PWR-VDD: Signal

SI (mm)	POWERSW_0	POWERSW_1	POWERSW_2	POWERSW_3
SI (mm)	25	25	25	25
SI (mm)	25	25	25	25
SI (mm)	25	25	25	25



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080_PW_KABY LAKE-U42/U22(1)
081_PW_KABY LAKE-U42/U22(2)
082_PW_***
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085_PW_***
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088_PW_LOAD SWITCH
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090_PW_PROTECTION
091_PW_+NVVDD (1)
092_PW_***
093_PW_+FBVDDQ
094_PW_***
095_PW_***
096_PW_***
097_PW_
098_PW_***
099_PW_FLOW CHART
100_Power On Timing--AC mode

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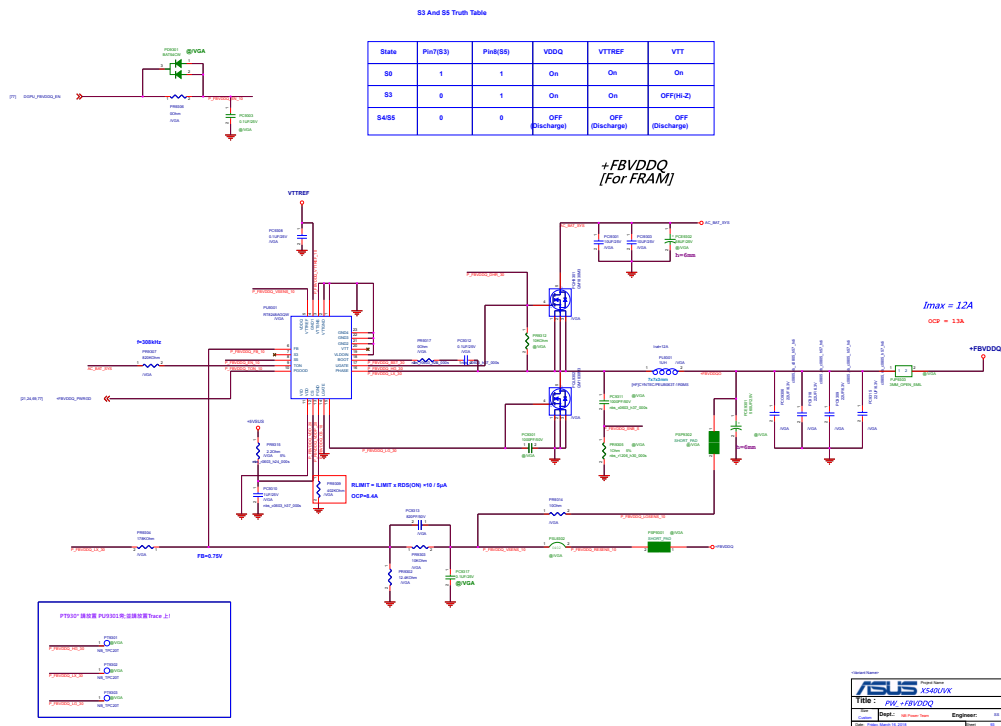
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080 PW KABY LAKE-U42/U22(1)

081_PW_KABY LAKE-U42/U22(2)

082_PW_***

083_PW_+1.0VSUS/+1.8VSUS

084_PW_

085_PW_***

086_PW_+1.2V/+VTT/+2.5V

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090 PW PROTECTION

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091 PW +NVVDD (1)
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092 PW ***

093 PW +FBVDDQ

094_PW_***

095 PW ***

096 PW ***

097 PW

098 PW ***

099 PW FLOW CHART

100_Power On Timing--AC mode

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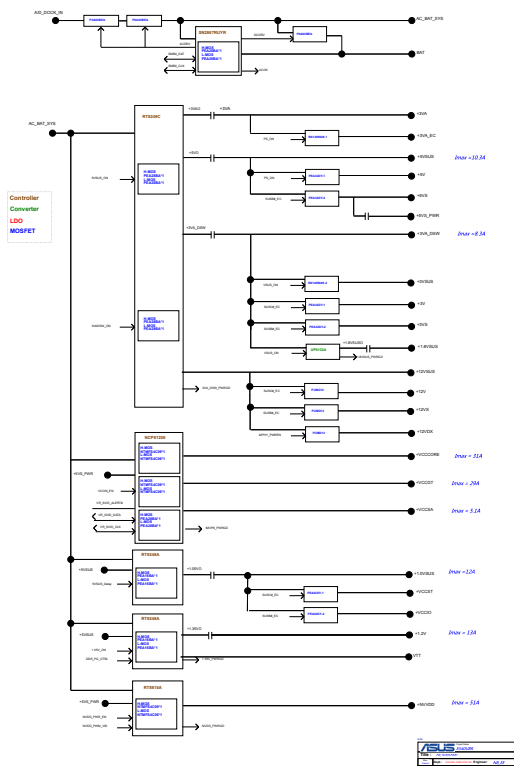
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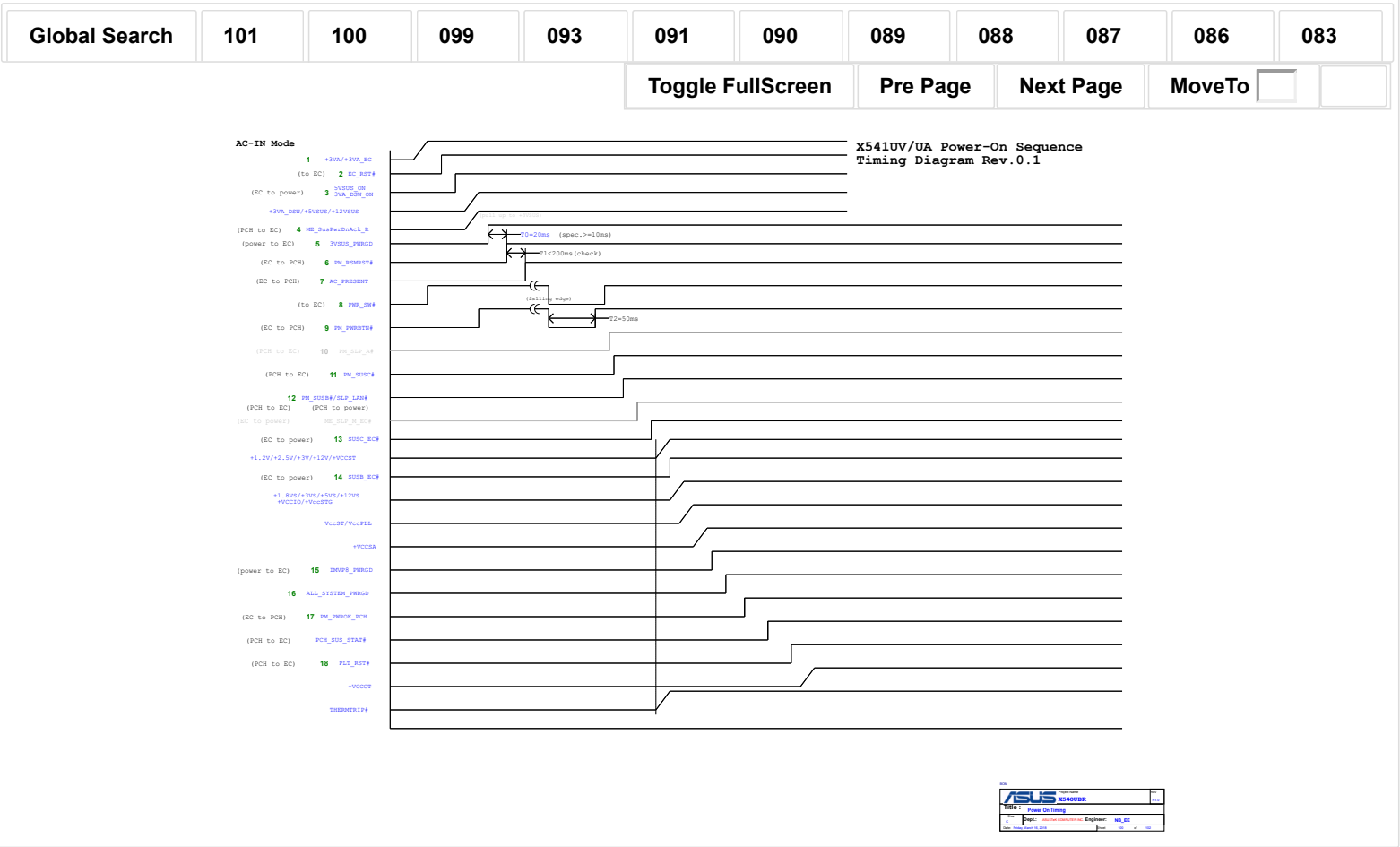
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080_PW_KABY LAKE-U42/U22(1)	▲
081_PW_KABY LAKE-U42/U22(2)	
082_PW_***	
083_PW_+1.0VSUS/+1.8VSUS	
084_PW_	
085_PW_***	
086_PW_+1.2V/+VTT/+2.5V	
087_PW_+3VADSW/+5VSUS	
088_PW_LOAD SWITCH	
089_PW_CHARGER	
090_PW_PROTECTION	
091_PW_+NVVDD (1)	
092_PW_***	
093_PW_+FBVDDQ	
094_PW_***	
095_PW_***	
096_PW_***	
097_PW_	
098_PW_***	
099_PW_FLOW CHART	
100_Power On Timing--AC mode	▼



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081_PW_KABY LAKE-U42/U22(2)

082 PW ***

083 PW +1.0VSUS/+1.8VSUS

084_PW_

085_PW_***

086_PW_+1.2V/+VTT/+2.5V

087_PW_+3VADSW/+5VSUS

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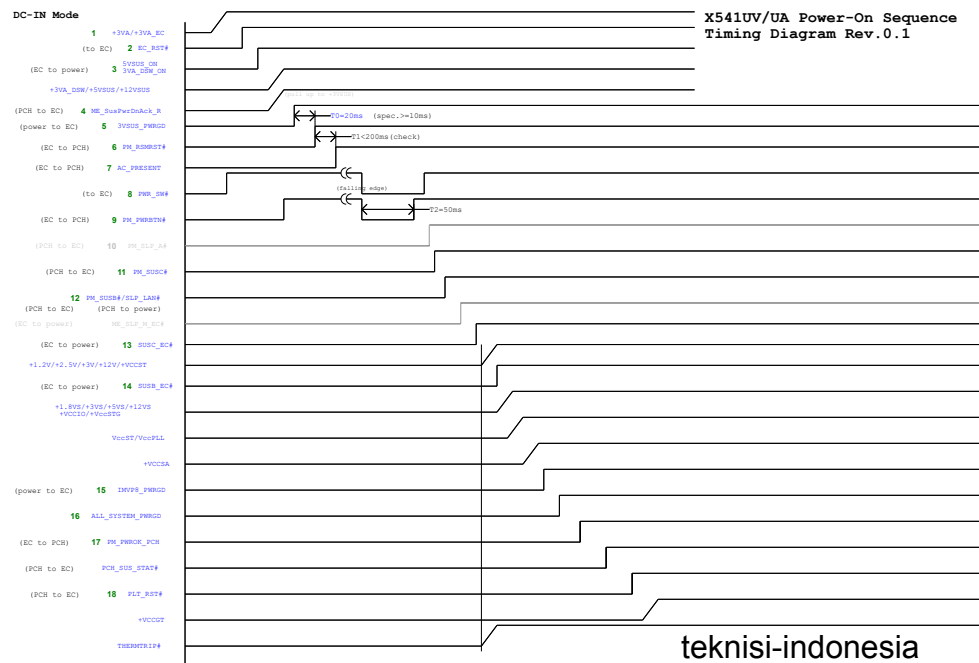
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